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FINAL REPORT
Contract No. DAAB07-76-C-0001 new

SUBJECT/KEY WORDS
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ABSTRACT/CONCLUSIONS

This is the Final Report of a 6 month study of duobinary digital data transmission over the DSCS. Analysis and computer simulations were developed for evaluating the degradation for duobinary SQPSK in the FDMA and TDMA modes, with emphasis on maximizing the bandwidth utilization capability of duobinary signalling. In a linear channel, single-access duobinary achieves rates of 3 bps/Hz, decreasing to 2.5 bps/Hz with a saturating transmitter and satellite. For duobinary FDMA, rates to 2.67 bps/Hz are possible in a nonsaturating channel with rates to 2.2 bps/Hz in a saturating channel. Error correction coding of duobinary is not recommended.

Duobinary modem considerations and implementations are discussed in depth. The modem should incorporate phase distortionless maximally-flat filters, a sampling detector, 4-bit quantizer, the Viterbi algorithm, modified sync and phase tracking loops, and (preferably) an adaptive equalizer. While a new modem design is recommended, modification of the Harris MD-1002 modem for duobinary SQPSK operation is possible, and the required changes are specified in detail.

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APPROVED BY: PROGRAM MANAGER _____ C. L. May _____ DATE: _____

DEPARTMENT MANAGER _____ C. R. Cahn _____ DATE: 6/28/77

⑥ PHASE DISTORTION STUDY (PHASE B)

FINAL REPORT

Contract No. DAAB07-76-C-0001

⑮

⑨ Final rept.

⑪ 30 Jun 77

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SECTION I
STUDY SURVEY AND KEY RESULTS

This report contains the results of the Phase Distortion Study (Phase B) performed for the U. S. Army Satellite Communications Agency by the Magnavox Government and Industrial Electronics Company. The major objective of this six month Phase B study was the further evaluation of the duobinary technique to improve bandwidth utilization for transmission of digital data over the Defense Satellite Communication System (DSCS).

As discussed in the Final Report[1], the Phase A study concluded that duobinary SQPSK has the potential for achieving a data rate of 3 bps/Hz of bandwidth in a linear channel. That is a 50 percent increase over the 2 bps/Hz capability of conventional SQPSK; furthermore, there is essentially no degradation in required E_b/N_o. Thus, the duobinary technique appears quite attractive for future application to the DSCS, where very efficient bandwidth utilization is an important goal for both TDMA and FDMA operation.

The objectives of the Phase B study include refining the duobinary signalling concept while evaluating the degradations which result from system impairments such as narrow bandlimiting, phase distortion, nonlinear amplification, AM-PM conversion, and adjacent channel interference. Also, duobinary modem implementation design considerations are addressed, including gain control for ternary modulation, channel filter characteristics, clock and phase tracking loops, and data detection, particularly where they differ from conventional modems. Decision-directed adaptive equalization for duobinary is also investigated.

In order to improve the bandwidth utilization over conventional SQPSK by the use of duobinary, the approach taken here is that of modifying only the receiver processing without changing the SQPSK modulation at the transmitter. With this approach, the necessary overall duobinary response is formed through the use of filters in the channel, with the option of an adaptive equalizer in the receiver. To optimize performance, a simple two-state Viterbi algorithm which exploits the redundancy in the waveform structure of duobinary is utilized in the receiver.

Performance is evaluated by means of a time domain computer simulation which represents the overall duobinary digital communication system. Computer program SIMB was developed for this purpose and contains all the required system elements of the transmitters, satellite, and receiver. Using these simulations, the degradation resulting from the various system and channel impairments are evaluated parametrically to determine the sensitivity of duobinary transmission to the various distortions encountered.

Both single-access (TDMA) and FDMA scenarios are simulated. Applied to TDMA operation, the key criteria is to maximize the data rate through the channel without severe degradation. For FDMA, the desire is to space the signals as close together as possible, keeping distortion and crosstalk to acceptable levels. Both linear and saturating channels are considered for FDMA and TDMA of the duobinary signals; in addition, the use of soft or hard limiting in the transmitter is investigated.

Convolutional encoding/Viterbi decoding is investigated for the duobinary SQPSK channel. Since duobinary has the objective of increasing the data rate in a given bandwidth while error correction coding decreases the rate, the two are in conflict, and the combined performance is examined carefully to determine whether the E_b/N_o reduction achieved with coding justifies the bandwidth increase and the increased complexity of the decoder. Since the same data rate results for either duobinary with rate-1/2 coding or conventional binary with rate-3/4 coding, both combinations of modulation and coding are compared with regard to performance and complexity of implementation.

This Final Report is divided into seven major sections, each pertaining to a specific topic addressed in the study. In addition there are five appendices, which contain supplementary information and supporting analyses developed during the investigation, including descriptions of the SIMB models and software.

The following results, based on this study, are of major importance to the system. Additional conclusions, recommendations, and areas requiring further investigation are given in Section VII.

- Uncoded duobinary SQPSK can achieve 3 bps/Hz with essentially no penalty in required E_b/N_o over nonsaturating channels. If the receiver has integrate-and-dump detection, the optimum filters for the transmitter and receiver have phase distortionless, maximally-flat characteristics.

- Rate-3/4 convolutional coding/Viterbi decoding of duobinary yields a relatively small coding gain (i.e., reduction in E_b/N_o). Rate-1/2 convolutional coding/Viterbi decoding of duobinary yields a substantial coding gain; however, transmission at the same data rate can be achieved with rate-3/4 coding of conventional SQPSK with an even lower E_b/N_o. Furthermore, the rate-3/4 Viterbi decoder for conventional SQPSK is a relatively simple modification of the standard rate-1/2 Viterbi decoder designed for the conventional binary channel. Since, in contrast, the Viterbi decoder for the duobinary channel is completely different and more complex than the standard Viterbi decoder, convolutional coding/Viterbi decoding is not recommended for use in combination with the duobinary channel. Instead, a capability for applying rate-3/4 coding with conventional SQPSK modems should be developed for the DSCS.

- Duobinary SQPSK is more sensitive to system phase distortion and AM-PM conversion than is conventional SQPSK. Decision-directed adaptive equalization, effectively removes the degradation due to the phase distortion but cannot effectively remove the effects of AM-PM conversion.

- Duobinary SQPSK is more degraded when accessing the Phase II or Phase III satellite TWT than occurs with conventional SQPSK. It is found that 3 bps/Hz can be achieved with 2 to 3 dB degradation with duobinary, compared to 2 bps/Hz with 1 dB of degradation using conventional SQPSK.

- For a hard or soft limited transmitter and satellite TWT, single-access duobinary TDMA requires filters with $BT_b = 0.4$ in the transmitter, satellite, and receiver. This condition implies TDMA with burst rates of 2.5 bps/Hz, an increase of 50% over the burst rate of 1.67 bps/Hz permitted with conventional SQPSK over the same saturating channel.

- With a linear, soft, or hard-limiting transmitter, system performance remains relatively constant over a wide range of TWT input backoff. This insensitivity to drive implies that uplink power control of the duobinary accesses for TDMA operation is not a critical adjustment.

- For duobinary FDMA in a linear channel, signal spacings as close as 0.75 times the first data null frequency are feasible with filters having $BT_b = 0.333$. This corresponds to an overall transmission efficiency of 2.67 bps/Hz. FDMA with conventional SQPSK and equalized filters with $BT_b = 0.5$ has a transmission efficiency of 1.8 bps/Hz. Thus, a 45 percent increase in bandwidth utilization is achieved for duobinary FDMA in the linear channel.

- Duobinary FDMA passed through the satellite TWT gives a transmission efficiency of about 2.2 bps/Hz, in contrast with an efficiency of 1.8 bps/Hz with conventional SQPSK. This implies a 25 percent bandwidth utilization advantage for duobinary FDMA in the satellite channel. Duobinary, however, requires about a 3 dB larger TWT output backoff than conventional SQPSK for comparable degradation.

- If desired, the Harris MD-1002 SQPSK modem can be modified for use with duobinary SQPSK signalling. Required receiver changes include modification of the bit sync circuit to sample at the bit transitions with 4-bit quantization, elimination of the quadrupling loop and substitution of a decision-directed carrier tracking loop and sync zone detector, and addition of the duobinary Viterbi algorithm (which could be interfaced externally). The specific assemblies in the Harris MD-1002 modem which must be modified or replaced are identified in Appendix D.

- No modification is required to the transmitter. However, to form the duobinary channel response, a phase distortionless filter with a maximally-flat amplitude characteristic is needed in both the transmitter and the receiver. The design point for the filter is BT_b 0.4; however, a considerable variation in data rate from the design point can be tolerated.

1-4

SECTION II
DUOBINARY SIGNALLING TO IMPROVE BANDWIDTH UTILIZATION

This section studies the feasibility of improving bandwidth utilization by increasing the data rate of QPSK or SQPSK over a channel of restricted bandwidth. Applied to TDMA operation, this allows a higher burst data rate through the channel. Applied to FDMA operation, each transmitter and receiver can have a narrower bandwidth filter for a given data rate; hence, the frequency spacing between the FDMA signals can be reduced.

The increase in data rate is achieved as a consequence of applying the duobinary signalling concept[2]. The point of view adopted here is that of modifying the receiver processing without changing the QPSK or SQPSK modulation at the transmitter. Thus, when an adaptive equalizer is utilized in the receiver the error is defined to control the receiver so as to form the overall transfer function necessary for duobinary demodulation. As will be seen, this involves only minor changes from conventional operation with respect to the definition of error in the bit output samples and the operation of the delay lock loop to optimize the sampling time.

Since improved bandwidth utilization is necessarily accompanied by an increase in required signal-to-noise ratio, the study concentrates on evaluating probability of error as a function of E_b/N_o. Use of the Viterbi algorithm to reduce the required E_b/N_o by taking advantage of the inherent redundancy of duobinary is described and presumed throughout this study.

2.1 DUOBINARY CONCEPT

We begin by describing the basic duobinary signalling concept, which is a modification of conventional binary signalling. The speed advantage of duobinary over conventional binary is due to the controlled utilization of intersymbol interference. Although only two levels are transmitted, three levels are received. In the simplest form of duobinary the middle level at zero amplitude is interpreted as binary 1 (corresponding to a polarity transition in the transmitted signal) while the top and bottom levels are both interpreted as binary 0 (corresponding to no transition in the transmitted signal). Thus, duobinary demodulation has a similarity to differential decoding, and the data is transmitted after differential encoding.

Figure 2-1 shows the idealized overall channel transfer function and the impulse response for duobinary signaling. Conventional binary demodulation of the received signal would sample at the peak, in which case the adjacent bits displaced in time by T_b would introduce significant intersymbol interference. Duobinary demodulation displaces the sampling time by $T_b/2$, and now there are three levels, $+2$, 0, -2, due to the controlled unit amplitude intersymbol interference from one adjacent bit only.
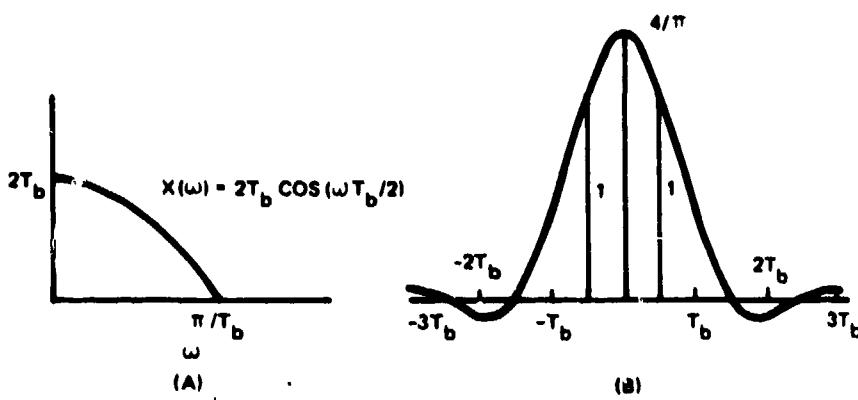
Figure 2-1. (a) Duobinary Filter and (b) Its Impulse Response

Assuming white noise in the receiver, the E_b/N_o degradation is computed in reference 2 to be 2.1 dB for this simplest form of duobinary when the idealized duobinary overall transfer function of Figure 2-1 is split equally between transmitter and receiver. However, with a sharp cutoff filter in the transmitter, the transmitted spectrum is approximately flat out to $\omega = \pi/T_b$; hence, the spectrum must be shaped for duobinary entirely in the receiver. Thus, for amplitude levels 2d, 0, -2d in the bit output samples and noise density N_o, we have

$$\text{Transmitted power} = S = \frac{d^2}{2\pi T_b} \int_{-\pi/T_b}^{\pi/T_b} d\omega = d^2/T_b^2 \tag{1}$$

$$\text{Noise power after receive filter} = \sigma^2 = \frac{N_o/2}{2\pi} \int_{-\pi/T_b}^{\pi/T_b} [2T_b \cos(\omega T_b/2)]^2 d\omega = T_b N_o \tag{2}$$

The distance to the decision threshold separating the levels is d; hence, the probability of error is characterized by the ratio

$$d/\sigma = \sqrt{ST_b/N_o} \qquad (3)$$

Since the probability of error for ideal binary transmission with conventional demodulation via a matched filter is characterized by the ratio $\sqrt{2ST_b/N_o}$, ideal duobinary spectrum shaping entirely in the receiver and demodulation based on the received amplitude levels entails 3 dB degradation in signal-to-noise ratio.

The duobinary concept is directly applicable to BPSK. It can also be applied to QPSK or SQPSK by combining two BPSK signals in phase quadrature, in the usual way. For QPSK, we assume independent differential encoding of the parallel I and Q bit streams, rather than mod-4 differential encoding, where the latter has the advantage of being invariant to a phase slip by 90°. The former is the only differential encoding applicable to SQPSK; however, the I and Q bit streams can be distinguished by their timing displacement of $T_b/2$. As a consequence, slips by 90° can be eliminated with SQPSK operation, as described in Section 3.1.

Henceforth, only QPSK or SQPSK is discussed for duobinary signalling.

2.2   ADAPTIVE EQUALIZATION FOR DUOBINARY

The above discussion defines the ideal duobinary system as having a controlled intersymbol interference, where the received amplitude level is the sum of the present bit and the new bit, but no additional contribution from any other bits. An actual duobinary transmission system can be made to approximate the ideal system by means of adaptive equalization in the receiver. The distinction between conventional binary and duobinary then arises when the desired response of the channel is defined. For conventional binary, the desired response is 1 or -1 in accordance with the polarity of the present bit. For duobinary, the desired response is 1, 0, or -1 in accordance with the sum of the present bit and the new bit. *

---

*This normalization involves a scale factor of 0.5 chosen for convenience.

When the data is known to the receiver a priori as a training sequence, the desired response can be formed from the known bits as specified above. For on-line equalization, a decision-directed control may be employed. With conventional binary, the desired response is created from the output samples by hard decisions which quantize to unit amplitude and retain the polarities as received. Figure 2-2 presents this concept of control by the LMS algorithm[6] and also includes a delay-lock bit synchronizer for optimizing the sampling time midway between the bit transitions.

With duobinary, the desired response for on-line equalization by decision-directed control is formed from the output samples by duobinary hard decisions. That is, if the sample amplitude exceeds +0.5, it is quantized to +1. If the amplitude is less than -0.5, it is quantized to -1. Otherwise, it is quantized to 0. One additional modification is necessary to convert from conventional binary to duobinary. The optimum sampling time is displaced by $T_b/2$. Therefore, still using a delay lock bit synchronizer to track the bit transitions as with conventional

677-3891
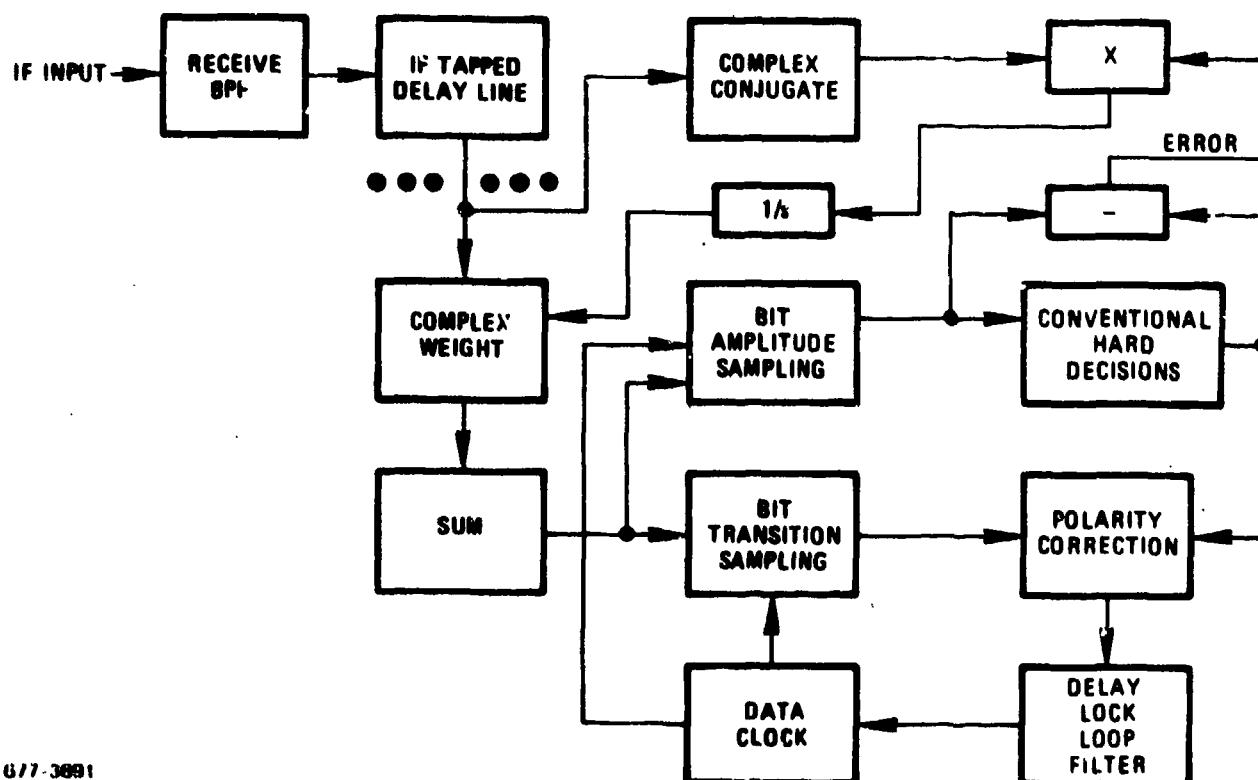
Figure 2-2. Adaptive Equalizer Concept for Conventional Binary With LMS Algorithm Control on Bit Amplitude Samples

binary, the sampling time is made to coincide with the bit transitions. Figure 2-3 presents the adaptive equalizer concept for duobinary operation. Note that the bit amplitude sampling is needed only for bit synchronization purposes. It is presumed that the data sequence is random so that a sufficient number of bit transitions are available for satisfactory operation of the bit synchronizer.
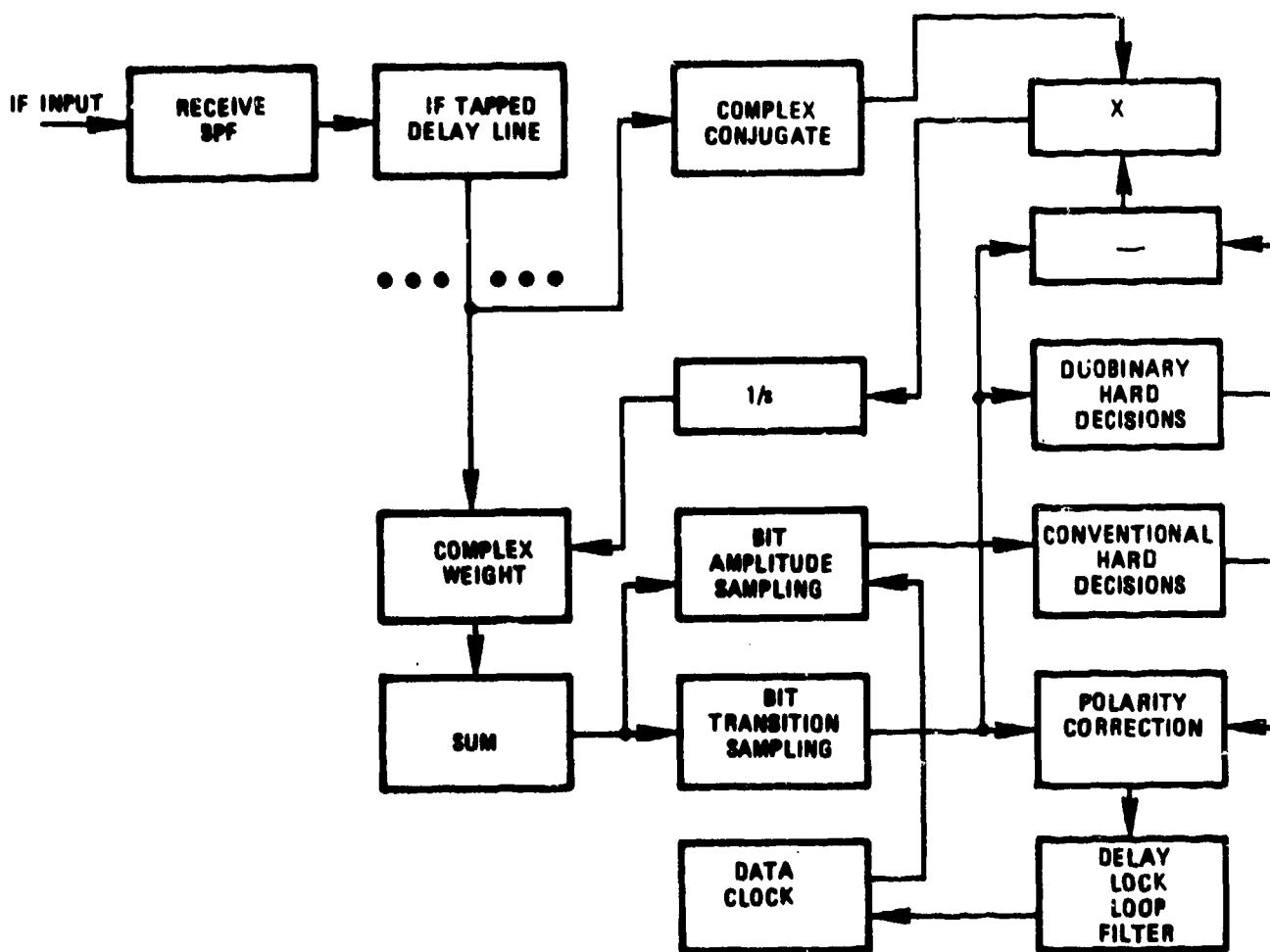
977-5193

Figure 2-3. Adaptive Equalizer Concept for Duobinary With LMS Algorithm
Control on Bit Transition Samples

MAXIMUM LIKELIHOOD DEMODULATION OF DUOBINARY BY THE VITERBI ALGORITHM

Section 2.2 has described the concept of applying an adaptive equalizer in the receiver to form a duobinary channel response, thereby increasing the maximum data rate for QPSK signalling through a narrow bandpass channel. However, in the simplest form, the required E_b/N_0 is degraded by approximately 3 dB, as a consequence of the ternary decision for duobinary demodulation. That is, if v denotes the sample amplitude (soft decision), which ideally would have one of the levels −1, 0, 1 in the absence of noise, the duobinary hard decision is

$$.5 < v \implies \text{No transition; } + + \text{ sequence}$$

$$-.5 < v < .5 \implies \text{Transition } ; \left.\begin{matrix} + & - \\ - & + \end{matrix}\right\} \text{sequences}$$

$$v < -.5 \implies \text{No transition; } - - \text{ sequence}$$

where the decision thresholds are midway between the ideal levels. With differential encoding, the + + and − − sequences of transmitted bits are both interpreted in the receiver as binary 0 for the data bit, while the + − and − + sequences are both interpreted as binary 1.

With duobinary demodulation, making a data bit decision on a single sample necessitates a ternary to binary mapping, and potentially usable information is inherently destroyed by this mapping. As an illustration of the redundancy of duobinary, the ternary decision gives an error detection capability. For example, a decision that .5 < v following a decision that v < −.5 in the previous sample is not consistent with the duobinary waveform; hence, an error has been detected (however, its location is still unknown).

The Viterbi algorithm* is a more sophisticated technique for exploiting duobinary redundancy for error correction, thereby decreasing the E_b/N_0 degradation of duobinary demodulation[3]. The algorithm assumes an ideal duobinary response, such that the channel output due to a single pulse has two sample values equal to 0.5 with the remaining samples being zero. Thus, intersymbol interference on a

---

*Note, this does not mean a Viterbi decoder for a convolutional code. As used here, Viterbi algorithm implies a recursive computation exploiting a finite set of system states to trace the optimum path yielding the maximum likelihood sequence. Viterbi decoding is discussed for duobinary in Section IV.

new pulse is due solely to the present pulse. Transmitting a sequence of pulses of amplitude ±1, a sample can take on one of the amplitudes .5 + .5 = 1, .5 - .5 = 0, or -.5 - .5 = -1.

The basis for the Viterbi algorithm is that the bit output sample (in the absence of noise) depends only on the present and the new pulse polarities. Therefore, the present pulse polarity specifies the present state of the channel, and for binary transmission, there are two possible states. The new state is specified by the polarity of the new pulse. Figure 2-4 gives the state transition diagram with associated correct output amplitude values (in the absence of noise).
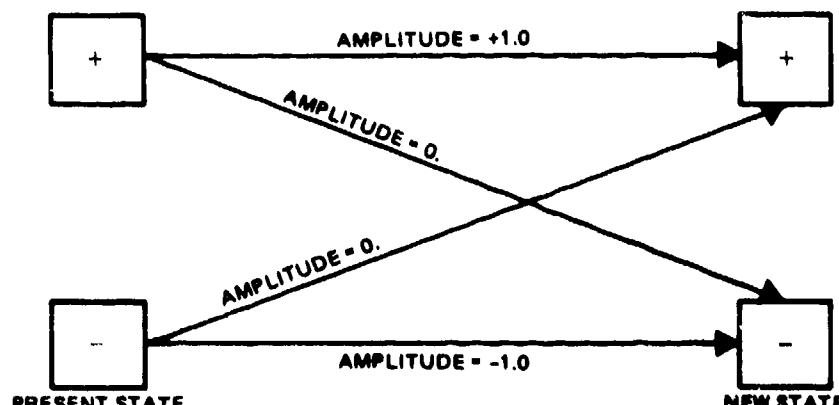
Figure 2-4. State Transition Diagram for Duobinary Channel

Presuming additive Gaussian noise for each sample, the log likelihood of a received amplitude v is $-(v-a)^2/2$, where a is the correct amplitude (see Figure 2-4). If the noise is independent from sample to sample, the log likelihood is additive and forms a metric for the Viterbi algorithm, where the objective is to find the sequence of states which has the maximum metric. However, only metric differences are needed; hence, we eliminate the common term $-v^2/2$. The resulting metric increment is given in Table 2-I, and shows how the soft decision v should be utilized by the Viterbi algorithm for duobinary.

Table 2-I. Metric for Duobinary Channel

| State Transition | | Correct | Metric |
Present	New	Amplitude	Increment
+	+	1.0	v-.5
+	-	0.	0.
-	+	0.	0.
-	-	-1.0	-v-.5

As usual[4] the Viterbi algorithm compares the metrics computed for the two possible paths leading to a new state, and only the higher metric is retained in storage for the new state. Also, this binary decision is then appended to the sequence of prior binary decisions on the retained path, and the new sequence is stored in the path memory for the new state. This comparison and updating process is performed for each possible new state. For the duobinary channel, there are just two states, and the Viterbi algorithm is quite simple. (The algorithm needs storage only for a single metric difference and a pair of path memories.) Figure 2-5 is a flowchart of the algorithm* (A similar algorithm is described in reference 5.)

The path memories introduce a decoding delay. The delayed quence of binary decisions from one of the path memories is differentially decoded to form the output binary data. Provided that the path memories are long enough, the two stored sequences will have remerged so that identical outputs would be obtained from either memory. (Slightly better performance would be achieved for a fixed decoding delay, where there is a non-zero probability of failure to remerge, by taking the output from the path memory of the state with maximum metric, but this is a refinement causing extra complexity.)

For QPSK, independent algorithms process the I channel and Q channel in parallel.

---

*The flowchart would be easier to follow if the two states each had a metric storage. However, as mentioned, only the metric difference needs to be stored. Figure 2-5 is a simplification of Figure 9-3 of the Phase A Final Report, and eliminates a path which cannot actually occur.

SOFT DECISION = V
METRIC DIFF = AM
PATH MEMORIES = I0, I1

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EXIT
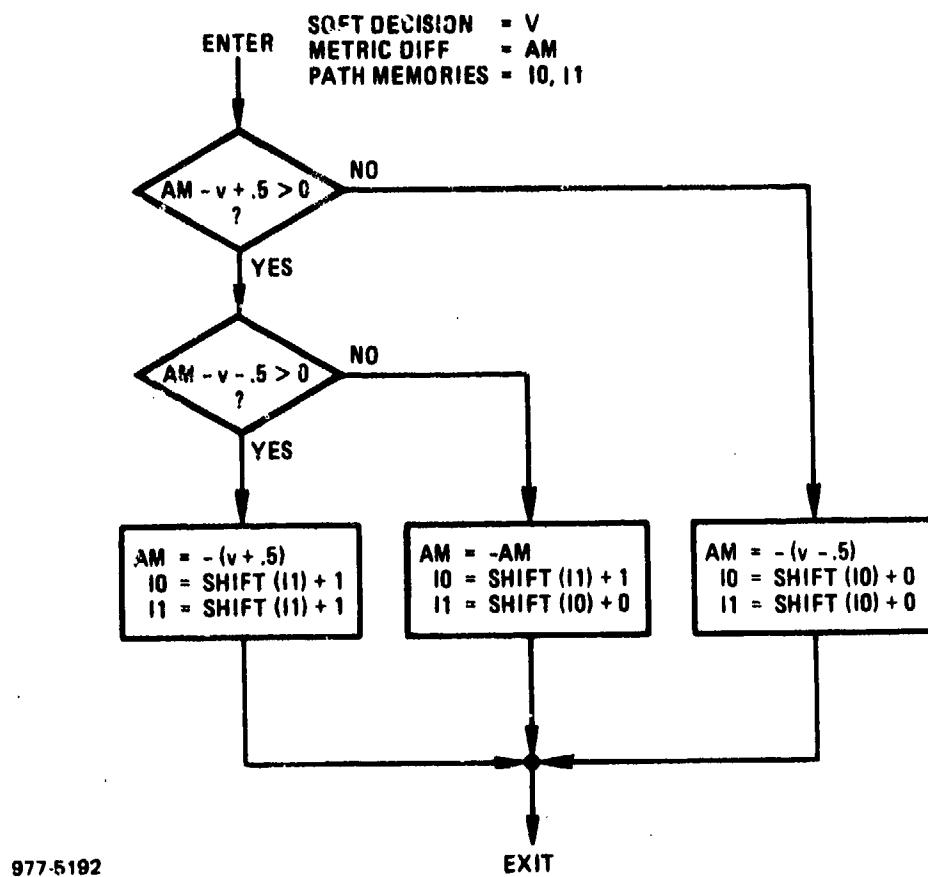
Figure 2-5. Flowchart of Viterbi Algorithm for Duobinary Demodulation

In a practical implementation of the Viterbi algorithm, the soft decisions must be quantized. With duobinary demodulation, the distance between zero amplitude and either the positive or the negative signal amplitude corresponds to the distance between positive and negative amplitudes for conventional binary demodulation. Since 3-bit quantizing is adequate for conventional binary, it is reasonable to quantize duobinary to 4 bits (16 levels) with the quantizer spacing set equal to the distance between the positive amplitude and the negative amplitudes divided by the number of levels (equal to 16). If the signal amplitude is unity, this yields a quantizer spacing of 0.125. Figure 2-6 plots the quantizer characteristic. Simulation results[12] for an ideal duobinary channel with quantization are plotted in Figure 2-7. With 4-bit quantization (N=8), performance is close to the unquantized case.
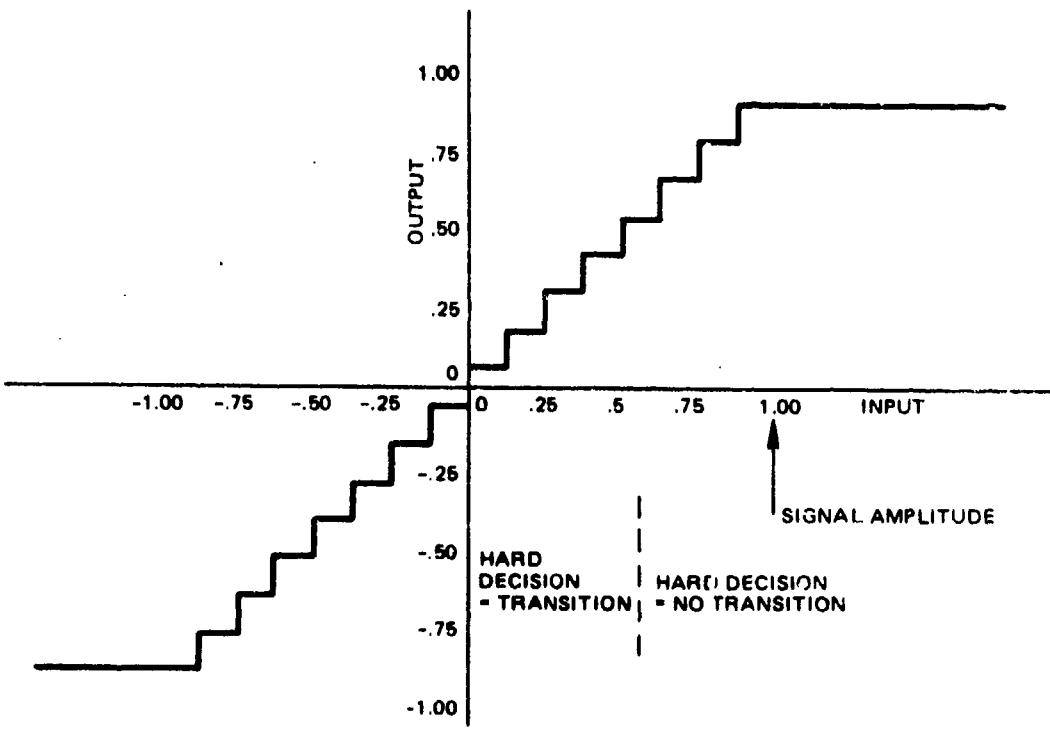
Figure 2-6. Soft Decision Quantizing for Duobinary
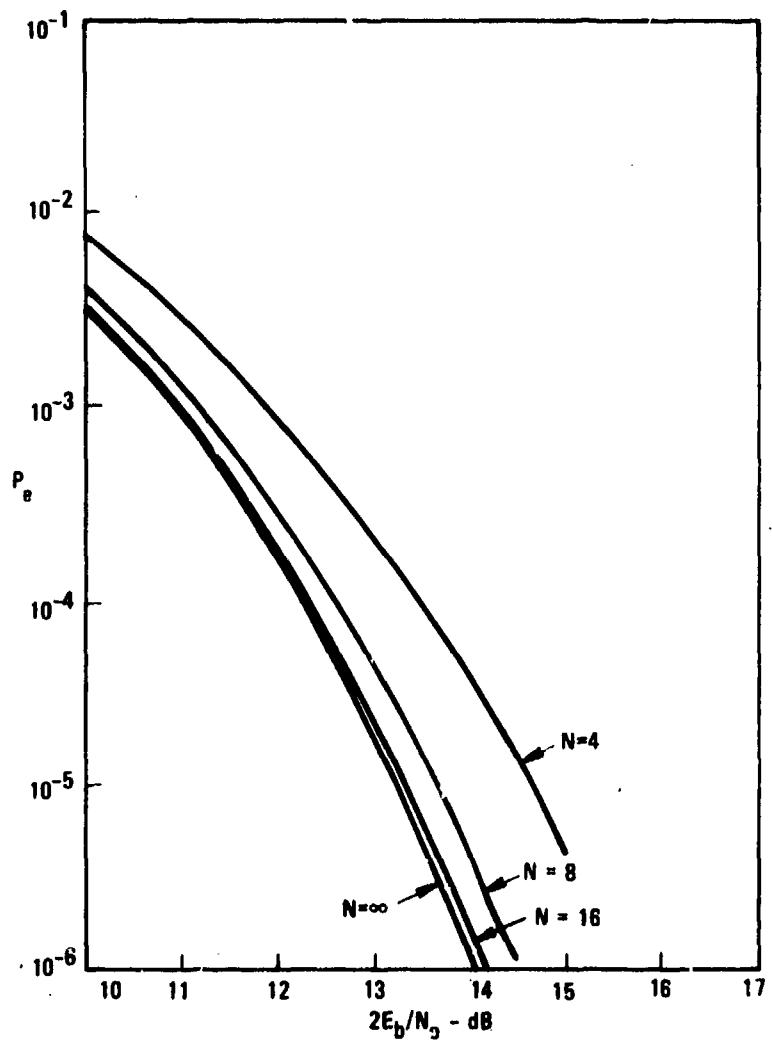
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Figure 2-7. Effect of Soft Decision Quantization on Duobinary Demodulation
(2N = Number of Levels from −1 to +1)

2.4 COMPUTER SIMULATION MODEL FOR DUOBINARY

The computer simulation model described in Appendix A for duobinary is a modification and evolution of that described in the Phase A Final Report. It incorporates the Viterbi algorithm correction routine as depicted in Figure 2-5. The program causes the adaptive equalizer to form a duobinary response with tap weight control from the decision-directed error of duobinary demodulation at the E_b/N_o specified for equalization. This adaptive process is unchanged by the addition of the Viterbi algorithm. After convergence, the tap weights are fr en, and the bit transition samples from the equalizer output a e input to the Viterbi algorithm routine. The inphase and quadrature bit transition samples are taken as parallel independent streams, with parallel Viterbi algorithm correction, so that storage is necessary for four states.

In this simulation, the error rate can be directly measured by counting errors actually made by the Viterbi algorithm when noise is present at the E_b/N_o specified for data transmission. The output data is taken from path memory I0, which introduces a delay of 32 bits (the computer word length). As mentioned previously, the output from the path memory is differentially decoded to give the output data. However, excessive computer time is needed* if errors are counted when the error rate is low, say, less than 10^{-3}. Appendix C describes and validates a technique to estimate the probability of error of the Viterbi algorithm from a relatively short computer run without counting errors directly. Briefly, this technique measures the mean and variance of the metric difference for comparing the two paths leading to the correct state. An error is necessarily committed by the Viterbi algorithm if the metric difference has the wrong polarity so that the incorrect path is the survivor. By fitting a Gaussian distribution to the measured mean and variance, the probability of an incorrect metric comparison is approximated from the tail of this fitted distribution, and the error rate is thereby estimated.

2.5 DUOBINARY SQPSK PERFORMANCE IN BAND-LIMITED CHANNEL

This section presents the basic performance of duobinary SQPSK in a linear channel of restricted bandwidth. The band limiting is set by a 5-pole Butterworth filter in the transmitter, and an identical filter is placed in the receiver. The

---

*For conventional binary, the error rate is computed from the bit amplitude samples, as discussed in the Phase A Final Report, and the problem of excessive computer time does not arise.

E_b/N_o is defined at the receiver input, before receiver filtering, in terms of the signal power remaining after transmitter filtering. Figure 2-8 shows the system block diagram including a decision-directed adaptive equalizer and a Viterbi algorithm demodulator. Note that phase tracking is implicit in the adaptive equalizer, as an inherent property of control derived from mean-square error minimization.
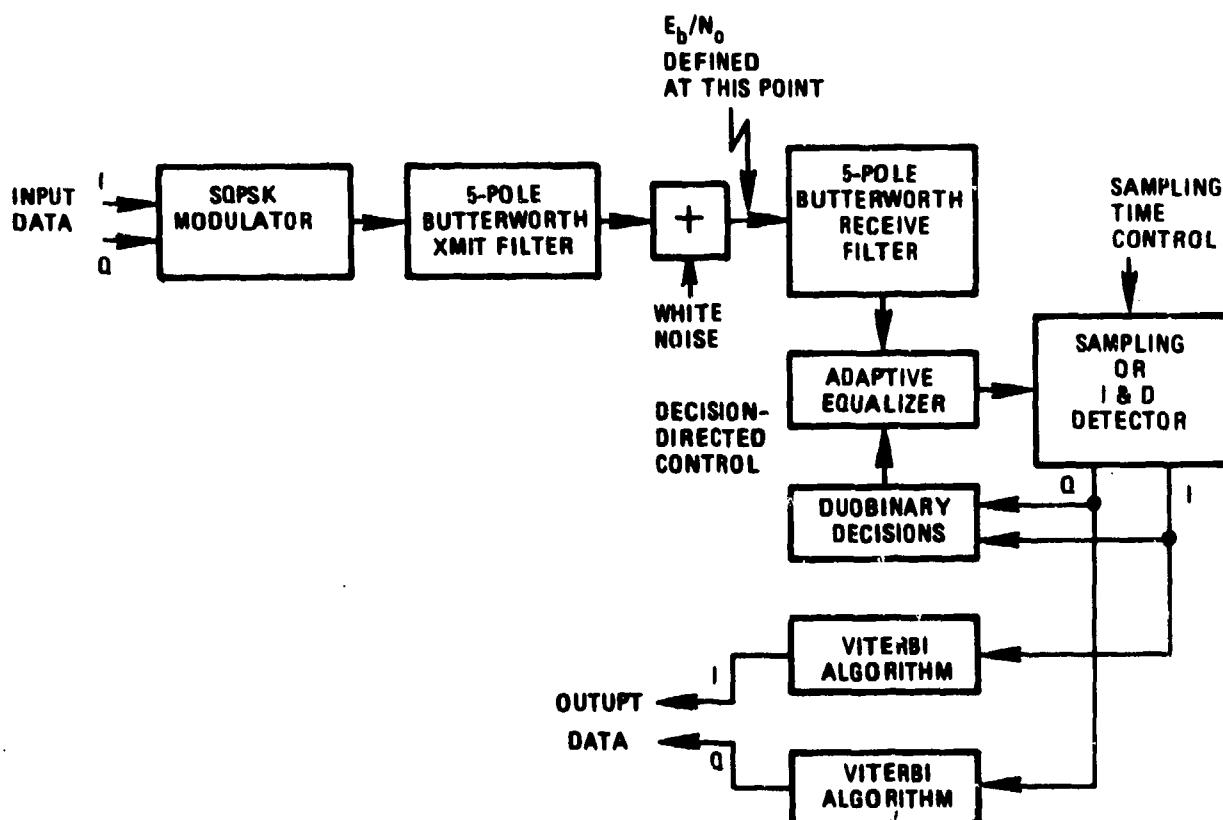
Figure 2-8. Block Diagram of Duobinary SQPSK System

The filter bandwidth is defined by the parameter BT_b, where B is the one-sided 3-dB bandwidth and T_b is the bit duration on the I channel. Thus, $BT_b = 0.333$ corresponds to QPSK or SQPSK transmission at 3 bps/Hz. Presuming a sampling detector, the channel response after adaptive equalization is given in Figure 2-9 for the overall frequency transfer function (two Butterworth filters and the equalizer). Note that the phase distortion due to the Butterworth filters has been removed almost completely, leaving a ripple of about 0.1 radian in the overall response. For comparison, the ideal duobinary response, Figure 2-1, is also plotted in Figure 2-9. The channel response in the time domain illustrating the transient for a single bit transition is plotted in Figure 2-10. Note that the amplitude is close to zero where the bit transition is sampled*, in accordance with the principle of duobinary operation.

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*Because of time quantization of the computer simulation to 1/16 of a bit duration, the zero crossing can be displaced slightly.
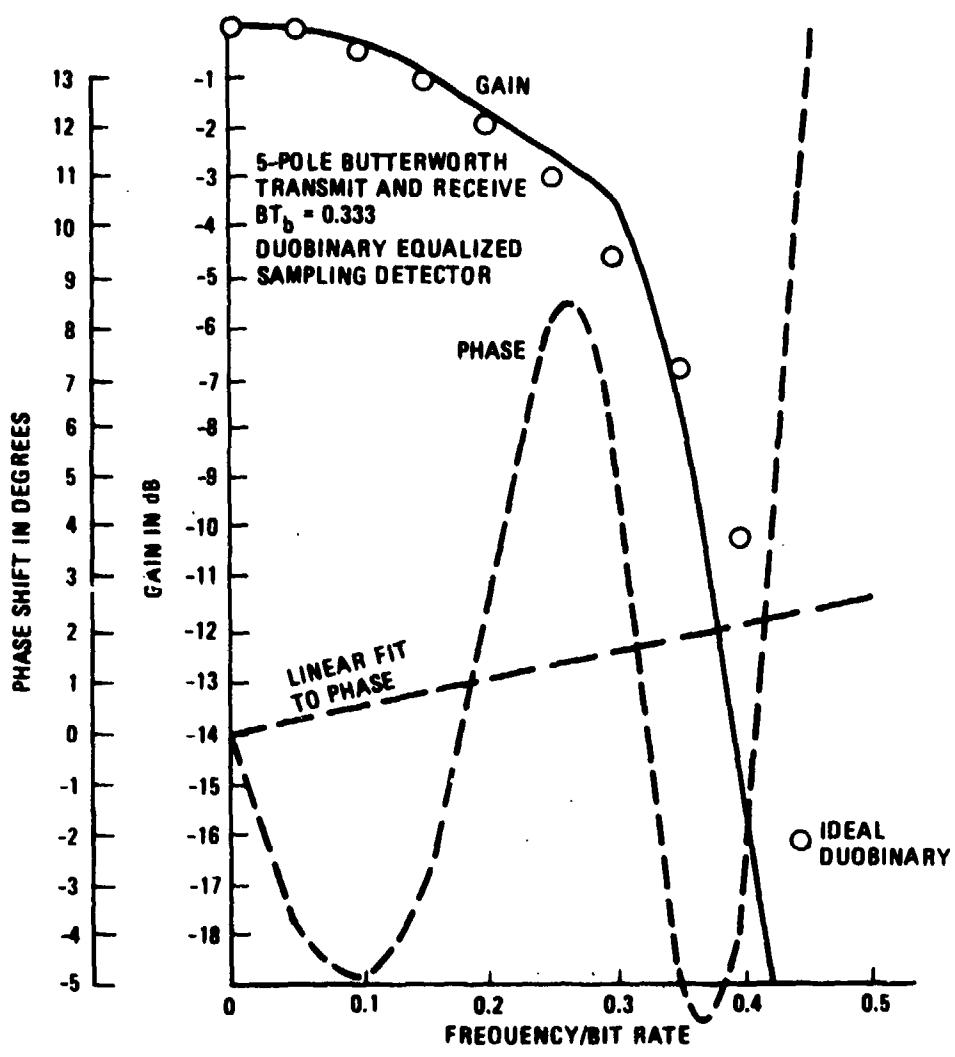
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Figure 2-9. Overall Channel Response, Duobinary Equalized

5-POLE BUTTERWORTH FILTERS, TRANSMIT AND RECEIVE CHANNEL EQUALIZED FOR DUOBINARY
$BT_b = 0.333$
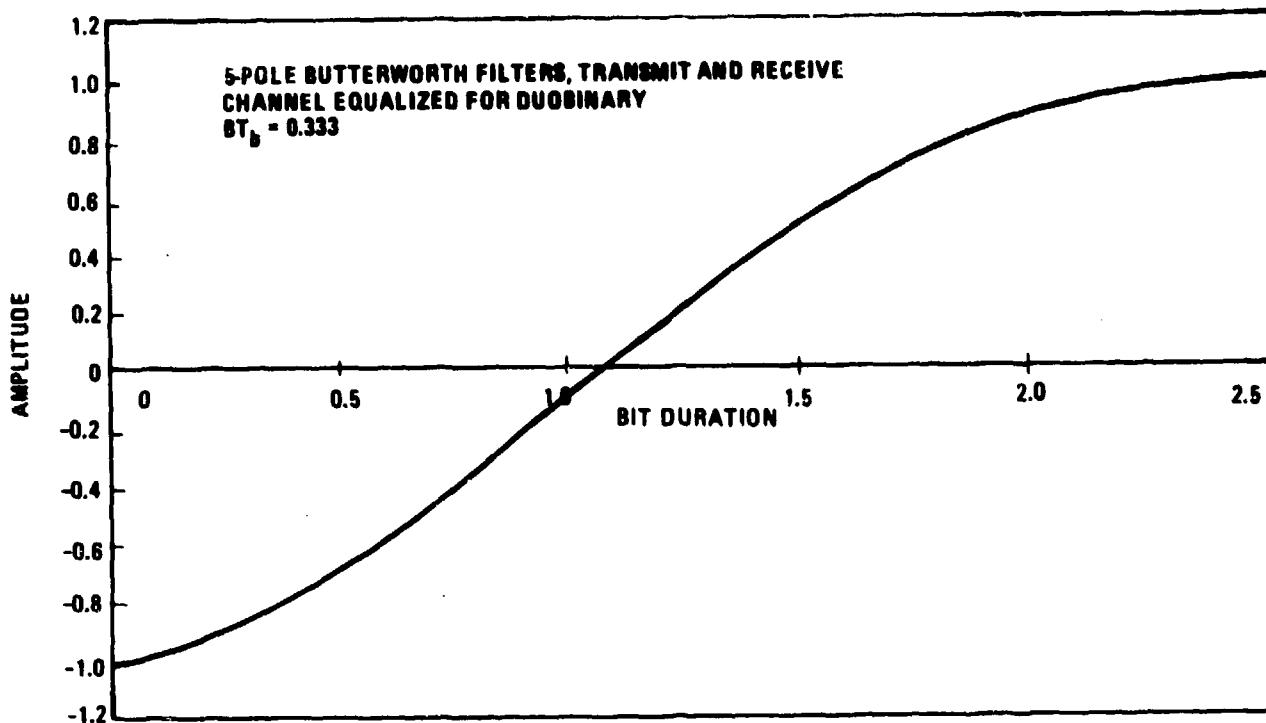
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Figure 2-10. Duobinary Channel Response to Single Bit Transition

Figure 2-11 presents the SQPSK duobinary performance (estimated from a total of 12800 bits) along with some error rate results by actual error counts taken from Figure 9-4 of the Phase A Final Report. Duobinary performance is evidently close to ideal differentially-encoded PSK, for SQPSK transmission at 3 bps/Hz. Although Figure 2-11 has been obtained for a sampling detector in the receiver, the results would be very similar with an integrate-and-dump detector, since the adaptive equalizer compensates for the detector's frequency response. Note that the integrate-and-dump frequency response, defined by $\sin(.5\omega T_b)/(.5\omega T_b)$, is down by only 1.6 dB at the cutoff of the Butterworth filter.

If maximally-flat, linear-phase filters are presumed instead of true Butterworth, the performance results with adaptive equalization will also be very similar to Figure 2-11, in view of the conclusion reached from Figure 2-9 that the equalizer acts to remove phase distortion in the channel.
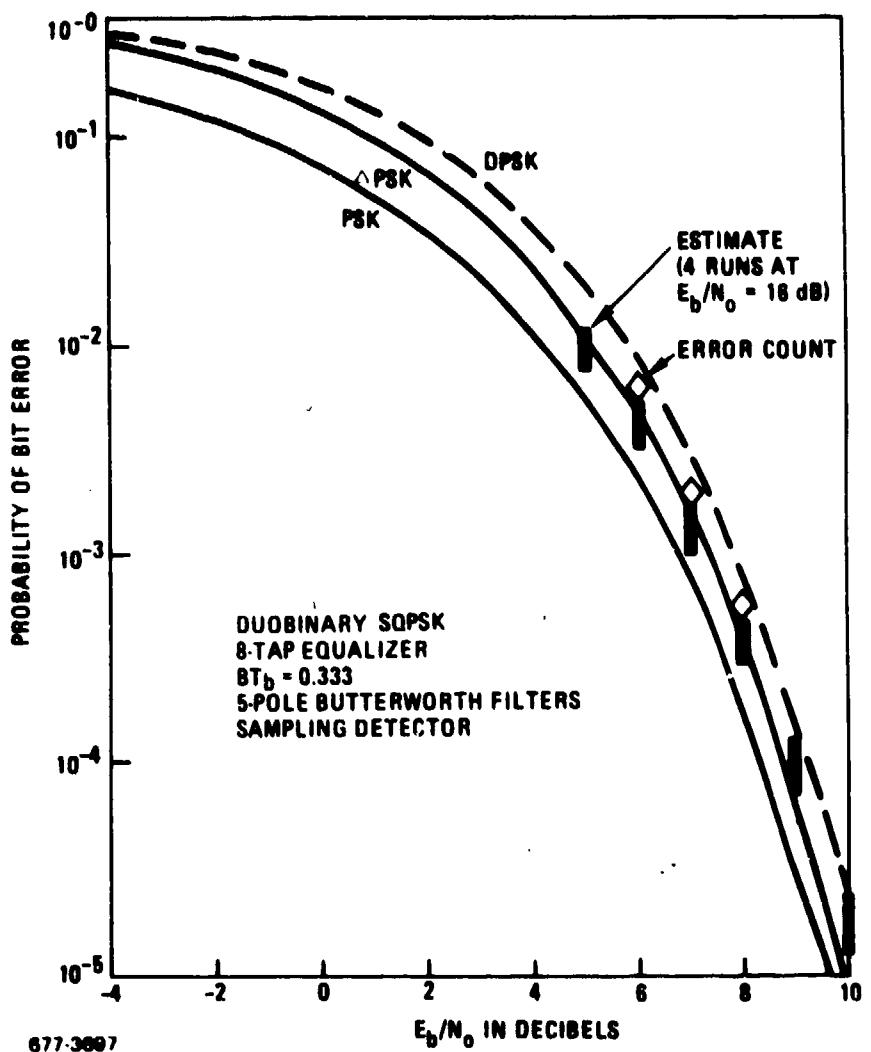
Figure 2-11. Performance of Duobinary SQPSK

2.6   DUOBINARY SQPSK PERFORMANCE IN CHANNEL WITH SOFT LIMITING

An important consideration concerning duobinary for satellite channels is its compatibility with saturation in the channel. Because of the envelope fluctuation due to narrowband filtering, duobinary SQPSK is more affected by channel nonlinearities than conventional SQPSK. For example, the discrete sidebands due to alternating data bits are at $\pm 0.5/T_b$, which lie outside the $BT_b = 0.333$ passband of the filter. Hence, after transmitter filtering, the output has a low amplitude in this case.

To study the effect of saturation, let us assume a soft limiting channel modelled with the error function characteristic

$$v_{out} = erf(A \, v_{in}) \tag{4}$$

where v_{in} is the input envelope (magnitude of complex sample), v_{out} is the output envelope, and A is a measure of input gain to adjust the output backoff (A ⟶ ∞ gives hard limiting, while A ⟶ 0 gives linear operation). There is no AM-PM conversion in this limiter model, so that the phase of the limiter output is identical to that of the limiter input. This nonlinearity is inserted in the system model of Figure 2-8 after the transmitter filter, and E_b/N_o is defined at the receiver input, as before. The receiver still incorporates a decision-directed adaptive equalizer, exactly as described in Section 2.5 for a linear channel.

Performance results from computer simulations (with estimated error rate) are summarized in Table 2-II, where the input gain is varied over a range from linear operation to hard limiting. Table 2-II gives the output backoff and the E_b/N_o required for 10^{-5} error rate, as functions of the input gain. Note that hard limiting causes a degradation of 4.4 dB in required E_b/N_o, compared to linear. An output backoff of 5 dB suffices to have linear channel performance.

Table 2-II. Duobinary SQPSK Performance With Soft Limiting, 3 bps/Hz, 10^{-5} Error Rate

Input Gain	Output Backoff	E_b/N_o	Saturation E_b/N_o
−20 dB	18.3 dB	10.4 dB	28.7 dB
− 6 dB	5.3 dB	10.4 dB	15.7 dB
− 1.4 dB	2.3 dB	11.1 dB	13.4 dB
0 dB	1.7 dB	11.3 dB	13.0 dB
+ 3.5 dB	0.7 dB	12.2 dB	12.9 dB
+ 9.5 dB	0.2 dB	13.7 dB	13.9 dB
∞	0.0 dB	14.8 dB	14.8 dB

Since using the full saturation output of a nonlinear amplifier can be viewed as a design goal for system operation, backoff from saturation represents a system degradation in the sense that the total available power in the channel is not fully exploited. The saturation E_b/N_o, defined as the sum (in dB) of the required E_b/N_o and the backoff, then should be viewed as the effective system performance. Thus, if the required E_b/N_o is reduced by 1 dB when the backoff is increased by 1 dB, the effective system performance remains unchanged according to this point of view. Table 2-II shows that duobinary SQPSK has an optimum backoff which minimizes the saturation E_b/N_o at approximately 13 dB for 10^{-5} error rate. Thus, with proper

adjustment of backoff, the effective degradation due to soft limiting of duobinary SQPSK is approximately 3 dB.

An important system consideration is the sensitivity to the gain control which adjusts the backoff. This is uplink power control with single-access operation, as in TDMA. Table 2-II shows that for the error function soft limiter model, the effective system performance remains constant within one dB over a range of input gain exceeding 10 dB (± 5 dB from a nominal setting). Thus, uplink power control for single access duobinary SQPSK operation in a saturating channel does not appear to require a critical adjustment. Further results presented later in Section 5.3.1 support this conclusion.

2.7   CONCLUSIONS

Duobinary SQPSK has the inherent capability of increasing bandwidth utilization without significantly degrading E_b/N_o, provided that a relatively simple Viterbi algorithm demodulator is utilized. The channel can be equalized by decision-directed control derived from duobinary hard decisions made on the bit output samples, which are taken at the bit transitions. Saturation in the channel, even hard limiting, can be tolerated with a degradation in required E_b/N_o, and uplink power control is not a critical adjustment.

SECTION III
DUOBINARY MODEM DESIGN CONSIDERATIONS

This section presents a detailed discussion of techniques for tracking carrier phase and sampling clock timing in a SQPSK modem designed for duobinary operation. To achieve performance approaching ideal, the duobinary modem requires narrowband transmitter and receiver filters properly shaped to produce an overall duobinary channel response. This is in contrast to a conventional modem with integrate-and-dump detection, where performance approaching ideal is attained in a wideband channel. The transfer function of the necessary filters for the duobinary modem is derived by controlling the tap weights of an adaptive equalizer to minimize the mean square error with respect to duobinary decisions on the output. Section 2.5 presented the resulting overall channel response where the filters are 5-pole Butterworth with $BT_b = 0.333$ prior to equalization, corresponding to transmission at 3 bps/Hz, and a sampling detector is assumed in the modem. If the modem has an integrate-and-dump detector instead of a sampling detector, adaptive equalization will compensate for the frequency response of the integrate-and-dump, so that the performance results in Section 2.5 still apply.

A receiver with an adaptive equalizer can compensate for carrier phase and clock timing offsets, and simultaneously correct phase and amplitude distortion in the channel. The modem of such a receiver needs only to have tracking loops which can lock to the carrier frequency and the bit rate, but without concern for the exact lock points maintained by the tracking loops. However, if the duobinary modem is operated with fixed filters, the exact behavior of the tracking loops must be ascertained.

The assumption is made throughout that the data stream is random. In common with conventional SQPSK, this implies sufficient bit transitions to ensure proper bit synchronization. Duobinary operation has the additional requirement that continual bit transitions should not occur, since this produces an output amplitude close to zero. * Under this condition, carrier phase tracking obviously would fail, since there is no signal available to track.

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*In this case, discrete sidebands offset by half the bit rate are produced, and they fall outside the channel bandwidth for duobinary operation.

An inherent characteristic of QPSK or SQPSK is an ambiguity in carrier phase tracking, such that lock up can occur initially to any of four stable tracking positions spaced by 90°. With QPSK, a carrier phase slip by 90° can subsequently occur; this interchanges the I and Q outputs (and complements one), but a mod-4 differential encoding* can be employed to eliminate any lasting effect from the slip. However, because of the displacement between I and Q sampling, SQPSK has information available to prevent 90° slips from persisting, provided that the clock timing does not drift as a consequence of the slip. Since a 180° slip still can occur, the data can be differentially encoded independently on I and Q to eliminate a lasting effect from the slip.

The following discussion on duobinary is restricted to SQPSK. The objective is to show how tracking information can be derived from the I, Q output samples of the modem to produce error voltages controlling carrier phase and clock phase. Also, techniques for gain control and detection of synchronization are described.

The motivation for the study is that a quadrupling loop, which successfully tracks carrier phase for conventional QPSK or SQPSK, fails on duobinary. The effect of narrow filtering is to cause the phase to deviate considerably from the ideal 0°, 90°, 180°, or 270°. As a consequence, after quadrupling the duobinary filtered SQPSK, the carrier component is quite small.

3.1   DECISION-DIRECTED CARRIER PHASE TRACKING

An approach to carrier phase tracking which works for duobinary can be derived from the LMS algorithm[6]. To begin, assume duobinary QPSK, and let a pair of inphase and quadrature output samples be represented by S (a complex number). A complex weight W is to be applied to S to yield the minimum mean square approximation to the desired output D (also a complex number). To optimize the system, the LMS algorithm increments the weight according to

$$\triangle W = K(D - SW)S*$$
(5)

*A logical table can be set up to convert the output bits back to the original data. This table is a function of the previous and the present pairs of bits.

where SW is the output, D−SW is the error, and K is a small constant setting the control loop bandwidth. If the weight is purely a phase shift, or $W = e^{j\theta}$, the increment in θ is approximately

$$\Delta\theta \simeq \frac{\Delta W}{jW} = -jK(D - SW)(SW')^* \tag{6}$$

Since θ is to be a real number, we use the real part on the right side of (6) yielding

$$\Delta\theta = K \, \text{Im} \left\{ D(SW)^* - |SW|^2 \right\}$$
$$= K \, \text{Im} \left\{ D(SW)^* \right\} \tag{7}$$

Equation (7) defines a carrier tracking algorithm which depends on knowledge of the desired output.

A decision-directed algorithm is obtained when the desired output D is derived from the actual output $SW = Se^{j\theta} = I + jQ$. Suppose the desired output is a quantizing performed on I and Q, specified by the function $D(v)$. Then, (7) becomes

$$\Delta\theta = K \left\{ -D(I)Q + D(Q)I \right\} \tag{8}$$

The right side of (8) is the restoring force to track carrier phase, and has the form of a cross product between the quantized I and Q and the unquantized I and Q amplitudes.

The extension of (8) to SQPSK is simply to compute the first term, $-D(I)Q$, at the inphase sampling instant and the second term, $+D(Q)I$, at the quadrature sampling instant, * which is displaced by one bit time, ** or $T_b/2$.

To track duobinary SQPSK, it is logical for $D(v)$ to be the three-level quantizing function for hard duobinary decisions, defined as

---

*A simple explanation of the alternating sign is that when the roles of I and Q are swapped at successive sampling instants, I is replaced by Q and Q by −I.

**In this section, bit time denotes the time between successive bits of SQPSK considered as a single serial data stream, while bit duration (T_b) refers to the I channel or Q channel alone.

$$D(v) = \begin{cases} 1; & .5 < v \\ 0; & -.5 < v < .5 \\ -1; & v < -.5 \end{cases} \tag{9}$$

An alternative is to treat the signal as conventional **SQPSK**, in which case the quantizing is hard limiting, or hard conventional binary decisions, defined as

$$D(v) = \begin{cases} 1; & 0 < v \\ -1; & v < 0 \end{cases} \tag{10}$$

The average carrier phase restoring force for a random bit sequence can be approximately computed with a periodic sequence of finite but reasonably long period. A carrier phase tracking loop will force the phase error to a null in accordance with this average restoring force. Figure 3-1 gives the average restoring force with $D(v)$ defined as (9), as computed for two different random bit sequences with a period of 128 bits and assuming the clock loop is tracking at its null (refer to Section 3.2). The carrier tracking loop pulls strongly to a phase error of either 0 or π; however, there are additional weak nulls which depend on the data sequence and would tend not to persist in the presence of noise. Note particularly the absence of a strong null at $\pi/2$.

Figure 3-2 plots the average restoring force with $D(v)$ defined as (10). Again, there is a strong null at 0 or π. Unexpectedly, the restoring force is inverted from Figure 3-1, so that the feedback to control carrier phase must be reversed to track correctly. It also appears that the null position in Figure 3-2 is somewhat more sensitive to the data pattern than in Figure 3-1.

3.1.1 EFFECT OF NOISE ON CARRIER PHASE TRACKING CHARACTERISTIC

One effect of noise on phase tracking is additive in nature and can be overcome by reducing the bandwidth of the tracking loop sufficiently. Here, we are concerned with the randomizing effect of Gaussian noise on the quantizer function $D(v)$, and thereby upon the shape of the average restoring force as a function of phase error.

677-3698
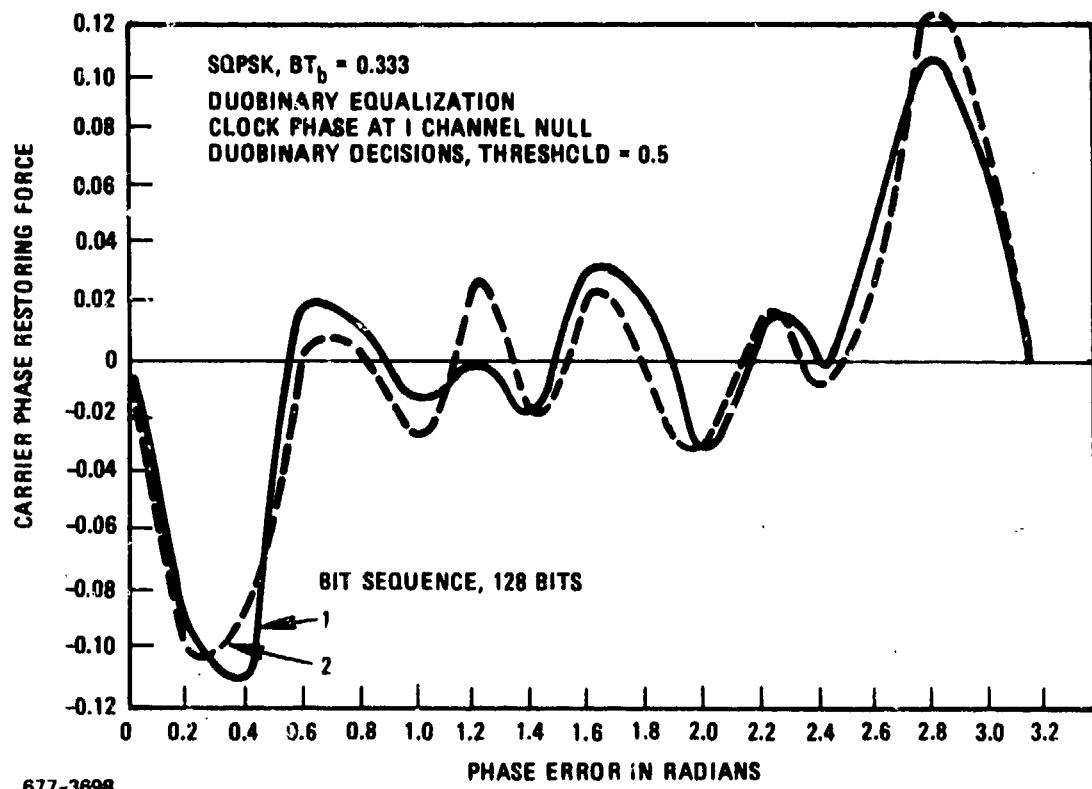
Figure 3-1. Decision-Directed Carrier Phase Restoring Force, Duobinary Decisions

677-3699
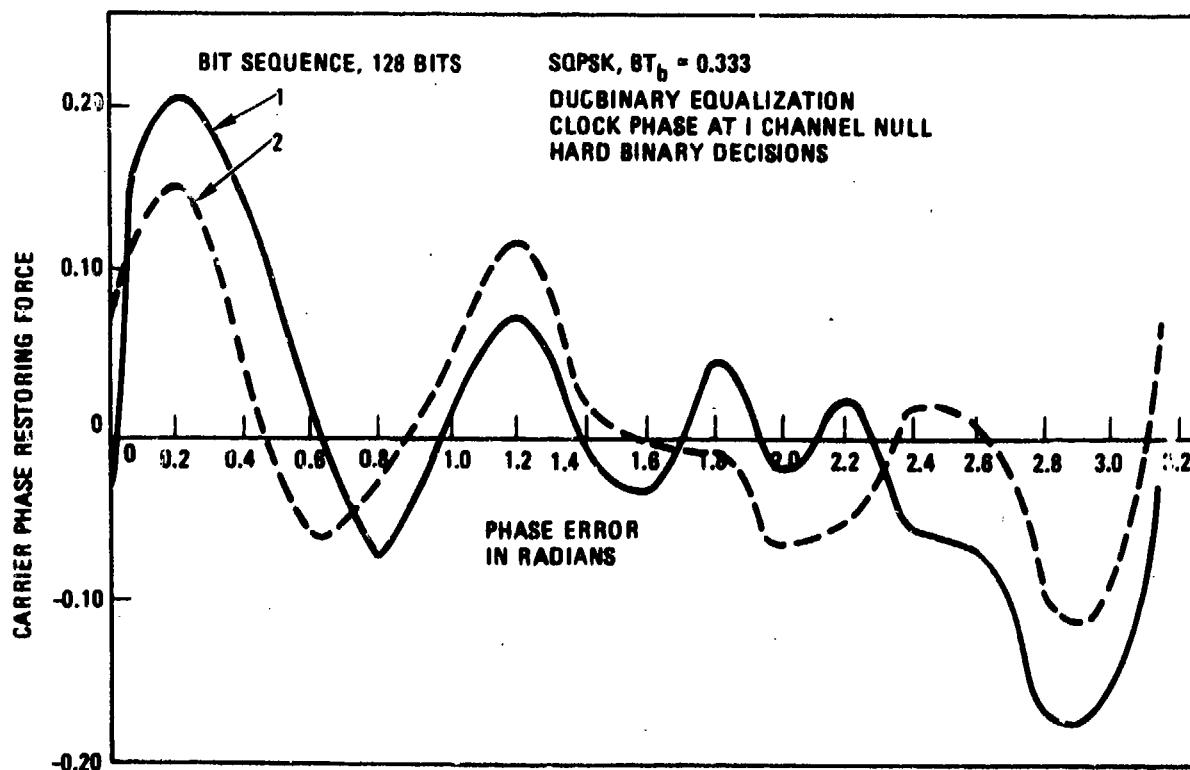
Figure 3-2. Decision-Directed Carrier Phase Restoring Force, Conventional
Binary Decisions

Since the noise voltages x and y added to the pair of I and Q samples taken at the same instant are independent Gaussian random variables, the expectation of (8) is easily computed. That is, the expectation of the product of independent random variables equals the product of the expectations; hence,

$$E\{D(I + x)(Q + y)\} \quad E\{D(I + x)\} \, E\{Q + y\}$$
$$E\{D(I + x)\} \, Q \tag{11}$$

noting that y has zero mean.

For D(v) given by (9), the expectation is

$$E\{D(I + x)\} = -\frac{1}{\sqrt{2\pi}\,\sigma} \int_{-\infty}^{-.5-I} e^{-x^2/2\sigma^2} \, dx + \frac{1}{\sqrt{2\pi}\,\sigma} \int_{.5-I}^{\infty} e^{-x^2/2\sigma^2} \, dx$$

$$= .5 \, erf\left(\frac{I + .5}{\sqrt{2}\,\sigma}\right) + .5 \, erf\left(\frac{I - .5}{\sqrt{2}\,\sigma}\right) \tag{12}$$

where σ^2 is the variance of the noise sample. Similarly, for D(v) given by (10), the expectation is

$$E\{D(I + x)\} = erf(I/\sqrt{2}\,\sigma) \tag{13}$$

Substituting the expectation of (12) or (13) for D(v) in (8), the average restoring force can again be computed. Figure 3-3 plots the result for $E_b/N_o = 7$ dB. (Note, σ is proportional to $\sqrt{N_o/2E_b}$, with the constant of proportionality determined by integrating the equalized response in the receiver.)

Comparing Figure 3-3 with Figures 3-1 and 3-2, it is seen that the slope of the restoring force at the null has been reduced somewhat by the effect of noise. The general shape of the restoring force characteristic has not been significantly changed, however.
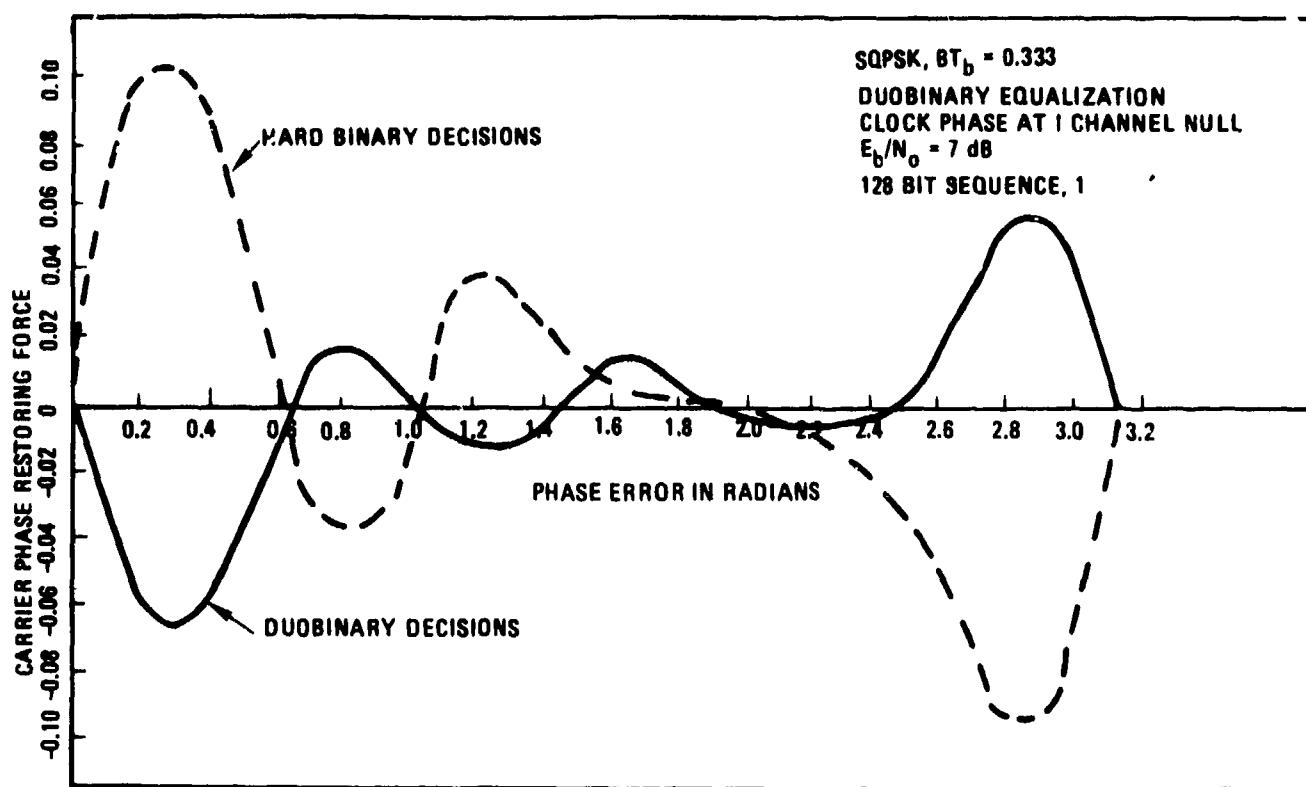
977-5194

Figure 3-3. Decision--Directed Restoring Force With Noise

3.2   CLOCK TRACKING

One approach to clock tracking for duobinary is to utilize the same scheme as for conventional binary; namely, the bit transitions are sampled and polarity corrected. The distinction between duobinary and conventional operation is that the bit amplitudes are sampled at the transitions for duobinary, but midway between the transitions for conventional. Thus, in principle, the same clock tracking circuit works for either, provided that the data sampling clock is offset to the transitions when converting from conventional to duobinary. The offset is one bit time at the SQPSK bit rate. (This is half the bit duration T_b on the I-channel alone.)

Figure 3-4 plots the average restoring force on clock timing (ignoring the effect of noise). One curve is for zero carrier phase error, and this shows where the clock tracking null occurs. * A second curve is for a carrier phase error of 0.4 rad, and shows that the clock loop will track correctly even for this carrier phase error. Of course, a carrier phase error of $\pi/4$ is the boundary beyond which the clock tracking null is displaced to the one bit time offset on the quadrature channel.

---

*Because of the time quantization in the simulation, the null does not occur exactly coincident with the instant designated to be zero in Figure 3-4.

CARRIER PHASE ERROR = 0 RAD

SQPSK, BT$_b$ = 0.333
DUOBINARY EQUALIZED 128 BIT SEQUENCE

0.4 RAD

CLOCK ERROR, BIT TIMES

CLOCK RESTORING FORCE
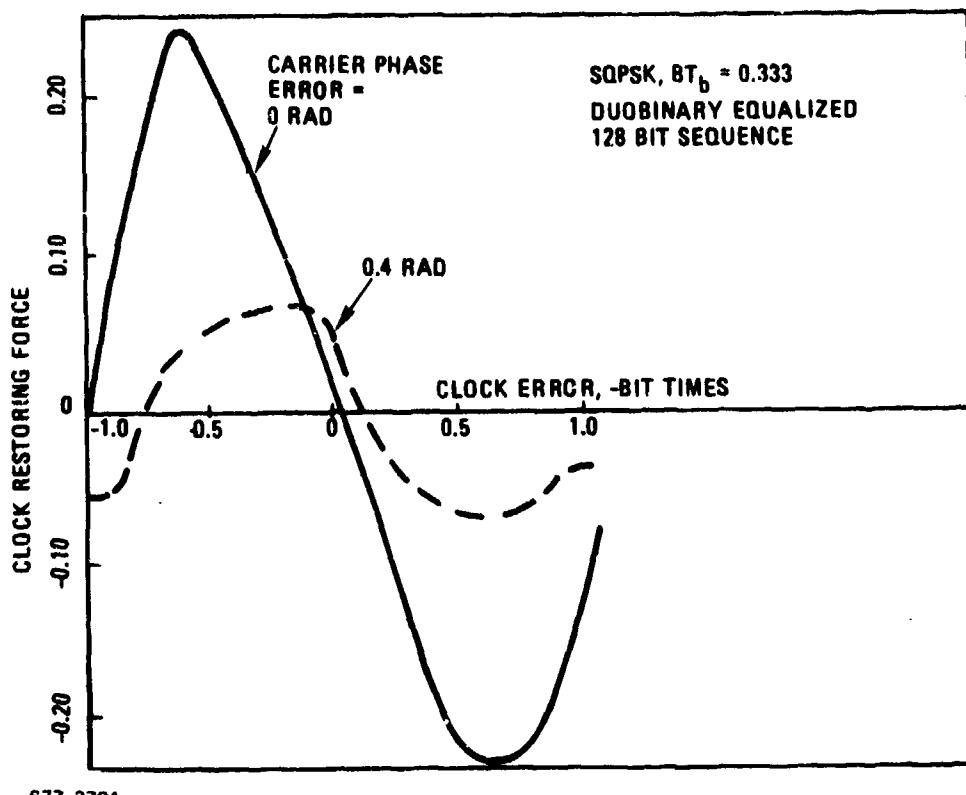
677-3701

Figure 3-4. Clock Restoring Force

Because the clock loop will pull toward the clock tracking null even with a substantial carrier phase error, we can expect the simultaneous carrier/clock tracking system to pull in from an arbitrary starting point, provided the carrier frequency error is not initially too large. A frequency sweep to ensure initial carrier acquisition can be employed to handle larger initial frequency errors. Conceptually, a sweep can be viewed as a staircase where the carrier frequency is stepped until sync is acquired.

3.3   SYNCHRONIZATION DETECTION AND GAIN ADJUSTMENT

To obtain the correct duobinary output, an accurate gain control is necessary. (In contrast, with conventional binary, gain control is necessary only to optimize the soft decision quantization for error correction decoding.) Gain control can be derived from duobinary decisions according to (9). That is, the average of all amplitudes exceeding 0.5 is controlled towards 1.0 by gain adjustment. Amplitudes below 0.5 are ignored for this control.

Taking a bit amplitude I with additive Gaussian noise x, and D(v) defined by (9), this amplitude averaging scheme yields the contribution

$$E\left\{(I+x)\ D(I+x)\right\}$$

$$= -\frac{1}{\sqrt{2\pi}\ \sigma}\int_{\infty}^{-.5-I}(I+x)e^{-x^2/2\sigma^2}\ dx + \frac{1}{\sqrt{2\pi}\ \sigma}\int_{.5-I}^{\infty}(I+x)e^{-x^2/2\sigma^2}\ dx$$

$$= .5I\left[\mathrm{erf}\left(\frac{I+.5}{\sqrt{2}\ \sigma}\right) + \mathrm{erf}\left(\frac{I-.5}{\sqrt{2}\ \sigma}\right)\right] + \frac{\sigma}{\sqrt{2\pi}}\left[e^{-(I+.5)^2/2\sigma^2} + e^{-(I-.5)^2/2\sigma^2}\right]$$

$$(14)$$

Similarly for a bit amplitude Q on the quadrature channel. The fraction of samples that have an amplitude exceeding .5 is

$$\mathrm{Prob}\left\{|I+x| > .5\right\} = 1 - \frac{1}{\sqrt{2\pi}\ \sigma}\int_{-.5-I}^{.5-I}e^{-x^2/2\sigma^2}\ dx$$

$$= 1 - .5\ \mathrm{erf}\left(\frac{I+.5}{\sqrt{2}\ \sigma}\right) - .5\ \mathrm{erf}\left(\frac{I-.5}{\sqrt{2}\ \sigma}\right) \qquad (15)$$

The behavior of this suggested gain control is evaluated by summing (14) and (15) over the sampled inphase and quadrature data amplitudes in a period of the bit sequence. The ratio then gives the average amplitude for all amplitudes exceeding 0.5. Figure 3-5 plots this average as a function of E_b/N_o. For $E_b/N_o > 0$ dB, the average varies by less than 5 percent.

Figure 3-6 shows how the average data amplitude can be used to control gain. The abscissa of Figure 3-6 is the actual gain, and the ordinate is the average of all amplitudes exceeding 0.5. There is a quite linear relation between the gain to be controlled and the resulting average amplitude.

Although Figures 3-5 and 3-6 have been computed for an averaging procedure, an essentially equivalent alternate procedure may be more easily implemented for an AGC loop. This alternate procedure is to average only the polarity of the difference between the data amplitude and the desired value of 1.0. (Again, amplitudes below 0.5 are ignored.) This AGC forces the median amplitude to 1.0.

3-9

677-3702
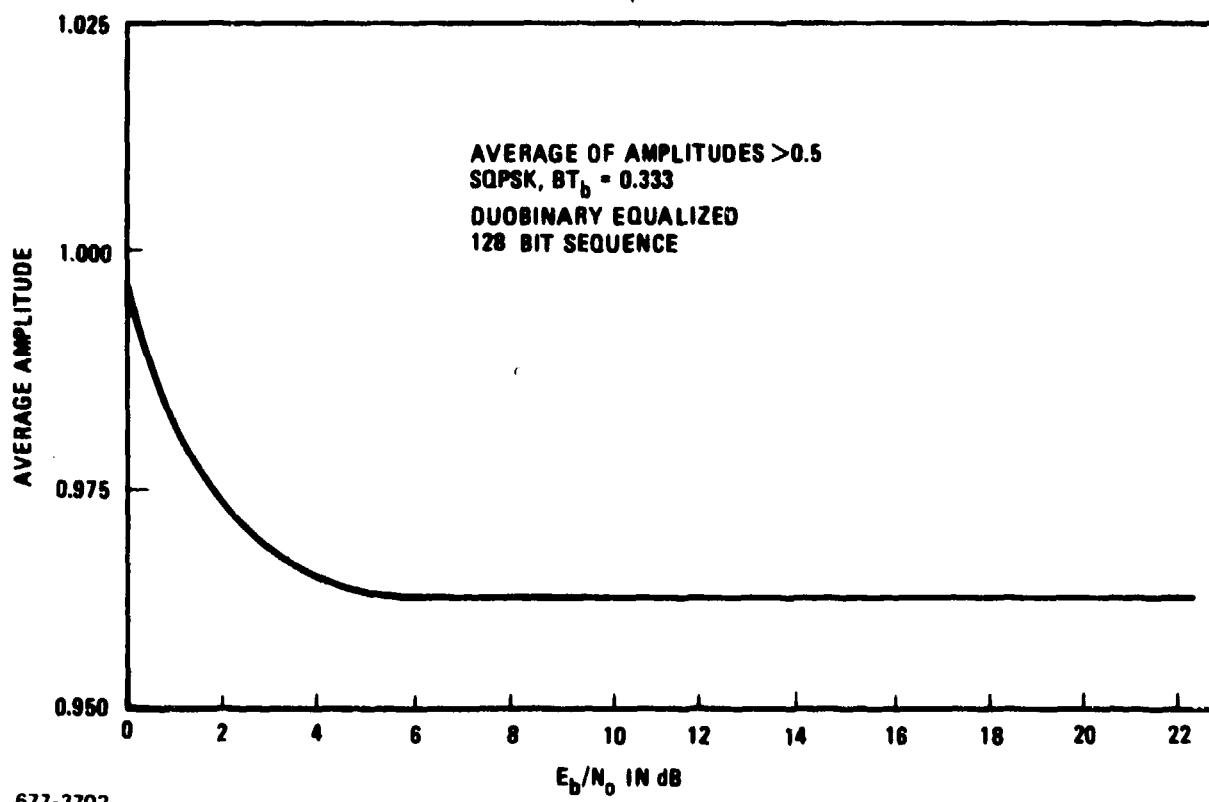
Figure 3-5. Average Amplitude Versus E_b/N_o

677-3703
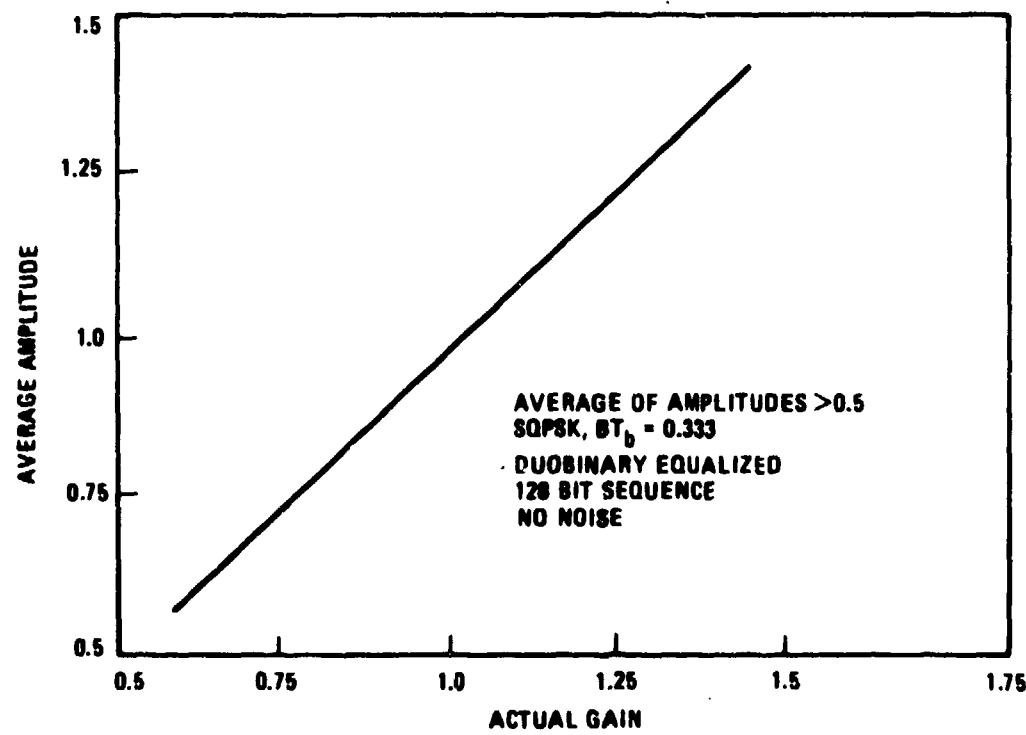
Figure 3-6. Average Amplitude as Function of Gain

The required accuracy of gain control can be assessed by measuring the probability of error of the Viterbi algorithm demodulator for duobinary. Increasing or decreasing the gain by 5 percent is found to degrade performance at P_e 10^{-5} by a few tenths of a dB. (P_e increases by a factor of about 2.) Thus, Figure 3-5 indicates adequate gain control accuracy for $E_b/N_o > 0$ dB.

The fact that gain must be controlled accurately for proper operation of the Viterbi algorithm for duobinary also enables a duobinary QPSK or SQPSK sync detector to be implemented. Since the duobinary output data amplitudes ideally are -1, 0, 1, sync can be recognized when the actual output data amplitudes cluster in the vicinity of these ideal amplitudes. As a reasonable design, the range of acceptable amplitude is set at ± 0.2; this corresponds to 1σ of noise at $E_b/N_o = 7$ dB. Then, noise causes the data amplitude to fall in the acceptable range with probability 0.68, at E_b/N_o 7 dB. Making a sync decision of $+1$ when the amplitude falls inside the acceptable range and -1 otherwise, the average of these sync decisions is found to be negative unless the receiver tracking loops are locked correctly.

3.4   BEHAVIOR OF COMPOSITE TRACKING SYSTEM

A simulation containing all the control loops described above demonstrates the feasibility of duobinary SQPSK tracking. The simulation includes carrier phase tracking, clock phase tracking, gain control, and sync detection, without additive n e.

The carrier phase restoring force is plotted in Figure 3-1 and displays a slope of approximately 0.5 in the vicinity of the tracking null at zero error. With ideal duobinary amplitudes of -1, 0, 1 and random data so that 0 occurs with probability 0.5, the slope would be exactly 0.5. The simulation has a second-order carrier phase tracking loop iterated at the SQPSK bit rate, and the (one-sided) noise bandwidth v of the loop is an input parameter.

The clock loop is first-order, iterated at the repetition rate of the periodic data sequence. At each iteration, the clock timing is advanced or retarded by one time quantum, in accordance with the polarity of the restoring force (see Figure 3-4).

gain control loop functions by comparing the absolute value of the sampled bit amplitude with the desired amplitude to obtain the amplitude error. If the bit amplitude exceeds 0.5, the desired amplitude is deemed to be unity and amplitudes below 0.5 are ignored for this control loop. The gain is adjusted proportional to the amplitude error to give a first order loop, the iteration

3-11

rate being the data rate. The gain control loop bandwidth is set equal to the bandwidth for carrier phase tracking.

The sync detector quantizes the amplitude error to +1 if the absolute value of the error is less than 0.2 and -1 otherwise. This quantity is smoothed in a first order loop with bandwidth equal to that for carrier phase tracking.

When the carrier and clock loops are tracking properly, the gain settles at 1.04, which drives the average amplitude to unity (see Figure 3-6). The sync detector builds up to almost unity (in the absence of noise), which means that all data amplitudes are within ± 0.2 of the ideal duobinary values (-1, 0, 1). However, if the carrier phase loop is not tracking, say because of excessive frequency error, the gain increases somewhat and settles down at 1.31, while the sync detector stays negative.

An example of the pull-in transient is plotted in Figure 3-7. There is an initial carrier frequency error of 10^{-3} rad/bit. Note that the clock loop at first pulls to zero error; however, the carrier phase error grows due to the initial frequency error. When the carrier phase error is in the vicinity of $\pi/2$, the clock is pulled towards the quadrature tracking position. Finally, the carrier loop acquires at zero error, although it could just as well have acquired at $\pi/2$. (This depends on the initial conditions.) The sync detector stayed negative until time unit 37, after which is rapidly rose towards 1.0.

Since there is no noise in the simulation, carrier phase tracking at a weak null could be observed for some initial conditions. The sync detector stays negative for this condition, however. As a further check, the simulation program was modified so that each successive 128 bit sequence is a new random sequence (rather than a repeat of the same sequence). It was found that after several 128 bit periods, the phase moved away from the weak null to a strong null.

With B_L/bit rate 10^{-3}, an initial frequency error of 2×10^{-3} rad/bit cannot be acquired. A linear frequency sweep of 5×10^{-7} rad/bit^2 can be acquired and tracked. (The carrier phase error settled to 0.13 rad.) For example, at a data rate of 100 Kbps, the loop bandwidth is 100 Hz and the sweep rate is $5 \times 10^{-7} \times (10^5)^2$ 5000 rad/sec^2, or 796 Hz/sec.
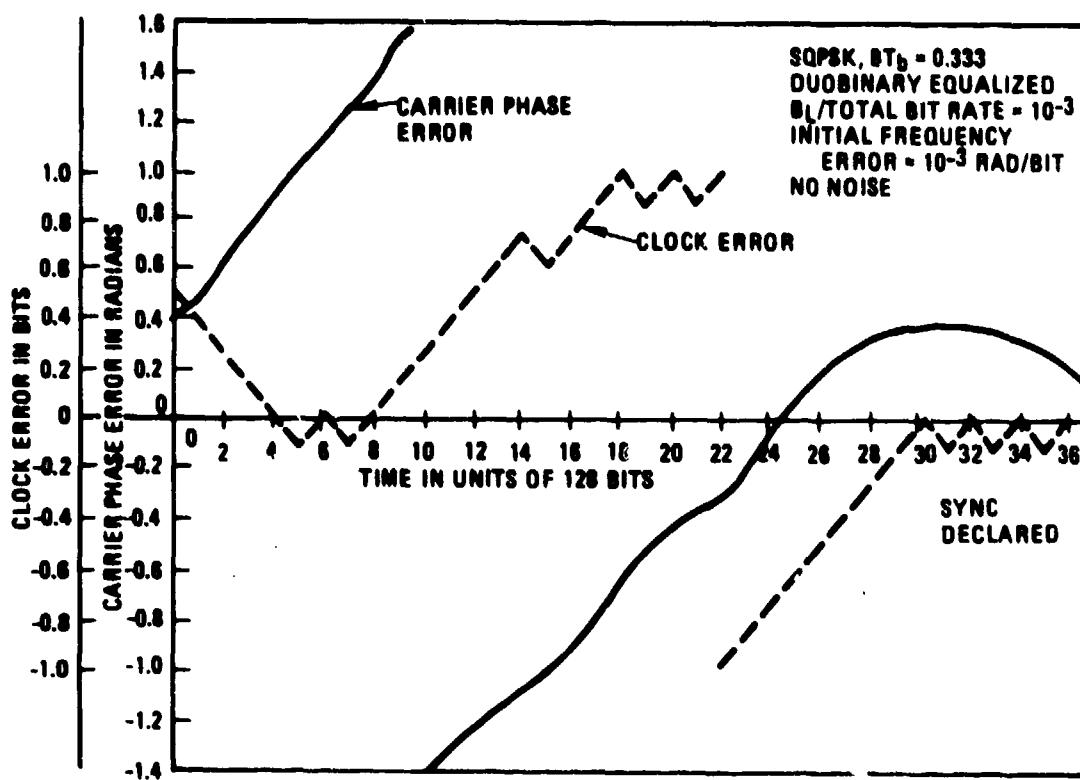
677-3704

Figure 3-7. Pull-In Transient for Combined Carrier Tracking and Bit Synchronization

3.5   OPTIMIZATION OF EXTERNAL FILTER FOR SQPSK MODEM MODIFIED TO DUOBINARY

This section assumes a SQPSK modem which has been modified for duobinary operation, with external filters in the IF to form the necessary overall channel response. The modem controls clock timing by a delay-lock tracking loop, and adjusts gain and carrier phase to minimize the mean square error with respect to hard duobinary decisions. A Viterbi algorithm demodulator is incorporated in the receiver to obtain the best possible duobinary performance.

A fixed filter can be designed to optimize modem performance at a specified data rate. However, to avoid excessive proliferation of filters in the operational system, it would be desirable that near optimum performance be achieved with a fixed filter over a range of data rates. Therefore, the effect of varying the data rate with fixed external filters is investigated.

The unmodified SQPSK modem is assumed to have an integrate-and-dump detector which is matched to the bit duration T_b. This yields ideal SQPSK performance when the data rate is much less than the channel bandwidth. The integrate-and-

3-13

dump detector is presumed to be retained when the modem is modified for duobinary. Note that the external filters can be designed to compensate for the integrate-and-dump response at a particular data rate. At other data rates, the variation of integration duration of the integrate-and-dump detector helps adjust the overall response; however, as will be shown, duobinary performance still is degraded when the data rate is much less than the channel bandwidth (in contrast to the situation for conventional binary in a wide bandwidth).

3.5.1 THEORETICAL DUOBINARY PERFORMANCE WITH INTEGRATE-AND-DUMP DETECTION IN WIDEBAND CHANNEL

To start with, consider the case where the channel bandwidth is extremely wide, so that the integrate-and-dump detector matched to the bit duration T_b is the only filter effectively present. As illustrated in Figure 3-8, the unmodified modem would sample at the peaks of the integrate-and-dump output, which are ± 1 yielding an ideal binary channel. The modem modified for duobinary has its clock timing displaced by $T_b/2$; hence, the samples are -1, 0, 1, also illustrated in Figure 3-8. This yields an ideal duobinary channel. The 0 amplitude occurs half the time with random data.

Note that the noise power added to the samples is the same for both clock timings, but the average power in the signal samples is unity for conventional binary and 0.5 for duobinary. This means performance is necessarily degraded by at least 3 dB for duobinary operation compared with conventional binary operation in the very wideband channel.
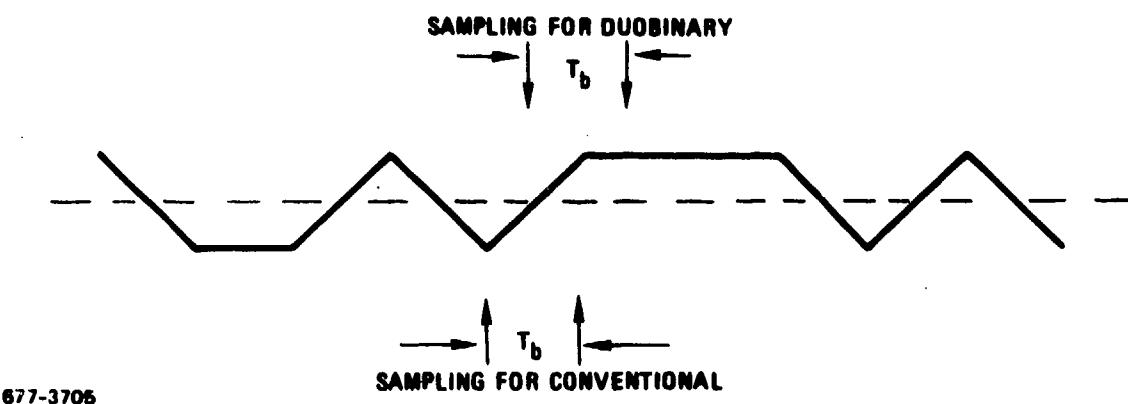
677-3705

Figure 3-8. Output of Matched Integrate-and-Dump Detector

3.5.2 DUOBINARY PERFORMANCE IN EQUALIZED NARROWBAND CHANNEL

Section 2.5 showed that duobinary SQPSK performance (with Viterbi algorithm demodulation) is close to ideal differentially encoded conventional binary when the channel bandwidth is narrow and a decision-directed adaptive equalizer forms an approximation to the desired duobinary response. Figure 3-9 plots the estimated performance, P_e versus E_b/N_o of duobinary SQPSK for two channel bandwidth values, assuming 5-pole Butterworth filters in both the transmitter and the receiver and an integrate-and-dump detector matched to the bit duration T_b. The performance for BT_b .333 is about the same as found previously for a sampling detector (see Figure 2-11) indicating, as expected, that the adaptive equalizer compensates for the integrate-and-dump response.
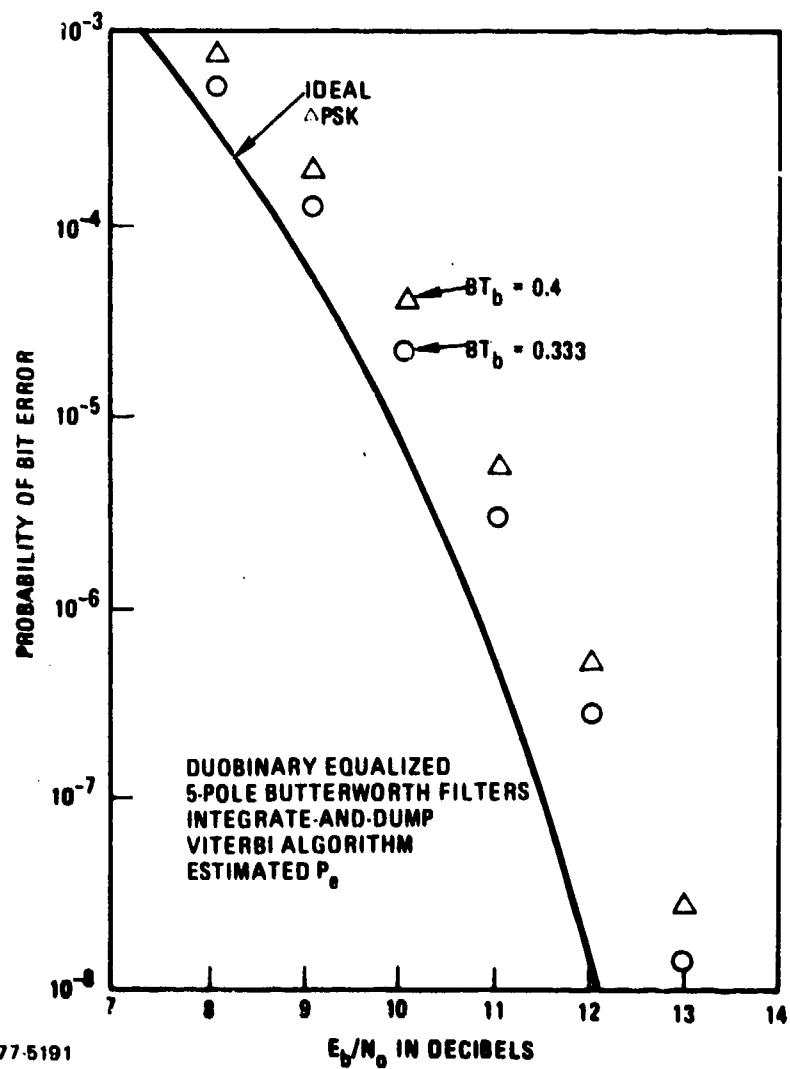
Figure 3-9. Duobinary SQPSK Performance in Narrow Bandwidth

Performance for BT_b .4 is a little poorer than for BT_b .333. (Remember that the adaptive equalizer minimizes the mean square error for the particular bandwidth value used.) If the bandwidth is narrower than BT_b .333, the performance again gets worse due to excessive intersymbol interference, despite the corrective action of the adaptive equalizer.

3.5.3 EFFECT OF VARYING THE DATA RATE WITH FIXED FILTERS

To reduce the number of different filters needed to operate over a range of data rates, a given filter can be designed to be optimum at a design value of data rate and used for other data rates near the design point. Consequently, suboptimum performance is accepted when the data rate deviates from the design point. The effectiveness of this approach is now evaluated for SQPSK duobinary with an integrate-and-dump detector in the receiver.

The transmitter and the receiver are assumed to have identical 5-pole Butterworth filters, with the bandwidth being an adjustable parameter. The data rate is fixed (or equivalently, the data rate is varied in a fixed bandwidth). Picking a specified bandwidth, a decision-directed adaptive equalizer in the receiver is allowed to converge to an approximation to the desired duobinary response. The resulting equalizer then is incorporated in the transmitter* as a transversal filter. Then, as the bandwidth is changed from the design point, holding a fixed data rate, the tap spacing of the transversal filter is stretched accordingly (inversely proportional to bandwidth), but the tap weights are unchanged.

At each bandwidth, clock timing is tracked by a delay-lock loop modified for duobinary so as to sample the integrate-and-dump detector output at the bit transitions. As suggested by (5), gain and carrier phase are controlled by having a one-tap "equalizer" in the receiver, with the single complex tap weight adjusted by the decision-directed LMS algorithm. Since symmetrical filters are employed, the carrier phase is expected to stay at zero, and this was found to be the case. The gain control is necessary because of the sensitivity of the duobinary demodulator to gain variation.

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*In a linear system, there is little difference in performance whether the equalizer is placed entirely in the receiver, entirely in the transmitter, or split between the two.

For each bandwidth, after the clock timing and the complex weight have converged, the probability of error for Viterbi algorithm demodulation of duobinary is estimated. The resulting degradation at E_b/N_o 10 dB is computed (i.e., the reduction in E_b/N_o to yield the same probability of error with ideal differentially encoded BPSK or QPSK). Results are plotted in Figure 3-10.

As expected, when the bandwidth is wideband, the degradation appears to be approaching 3 dB as theoretically predicted. When the bandwidth is narrowed below the design point, intersymbol interference becomes excessive and degrades performance. Nevertheless, the data rate can be varied considerably from the design point. Using the design point BT_b 0.4, the degradation at E_b/N_o 10 dB does not exceed 1.7 dB over the octave range of data rate from BT_b .31 to BT_b .62.

3.5.4   OPTIMUM EXTERNAL FILTER FOR DUOBINARY OPERATION

Selecting the design point $BT_b = 0.4$, the response of the corresponding external filter can be computed. It has already been shown in Figure 2-9 that the overall response has a linear phase after equalization. Figure 3-11 plots the amplitude response of the external filter presuming the equalizer is split equally between transmitter and receiver, each having a 5-pole Butterworth filter. As can be seen, the resulting filter has, very closely, a maximally-flat amplitude response. Thus, rather surprisingly, the equalizer functions only to remove the phase distortion of the Butterworth filters.

To demonstrate this, the computer simulation was modified to place linear-phase, maximally-flat filters in the transmitter and receiver. * Again, gain and carrier phase control is derived from a single complex tap weight adjusted by the decision-directed LMS algorithm. The (3 dB) bandwidth of the filters is an input parameter to the simulation. The estimated P_e versus E_b/N_o is plotted in Figure 3-12 for several different values of bandwidth/bit rate. The degradation is less than 2 dB at 10^{-5} error rate for bandwidths in the range $BT_b = .333$ to $BT_b = .666$. Note that the performance degrades rapidly when the bandwidth is narrowed further.

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*In a computer simulation, a zero phase filter is easily introduced in the frequency domain after FFT'ing the time samples.

677-3707
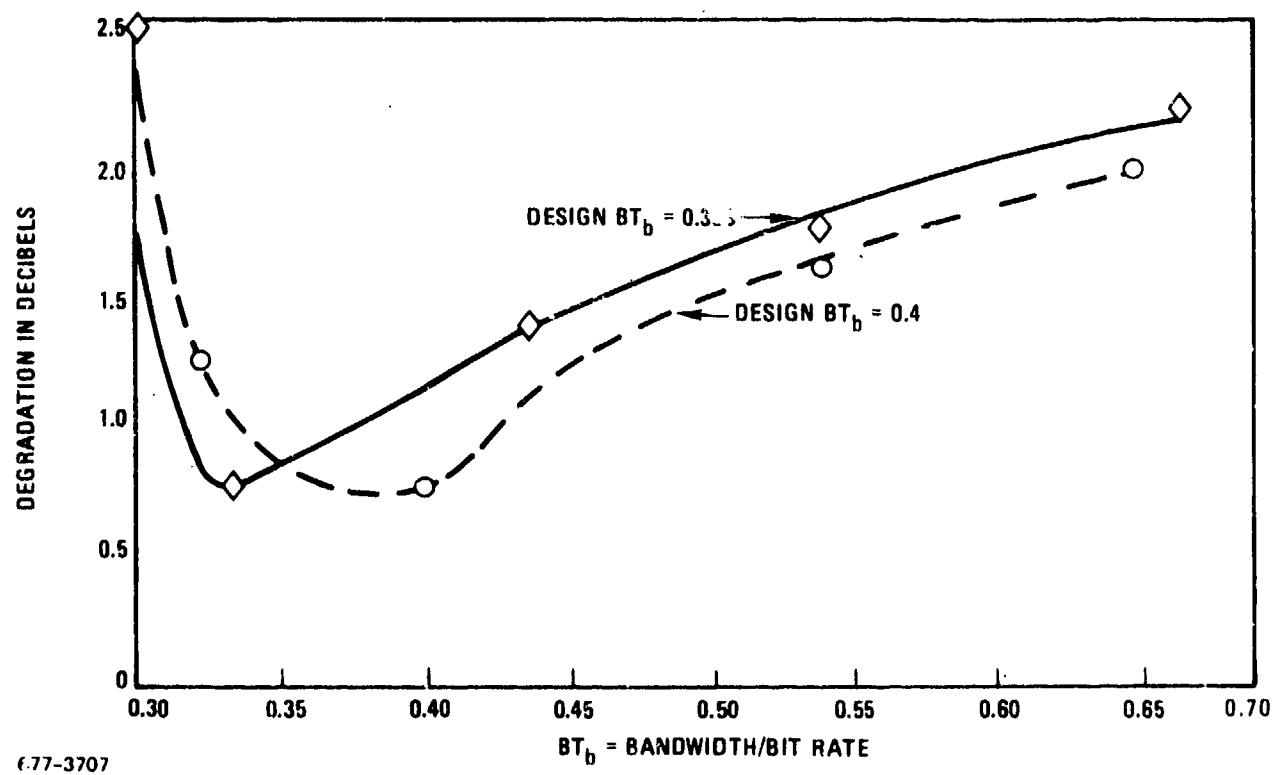
Figure 3-10. Duobinary SQPSK Performance With Integrate-and-Dump
Detector as Data Rate Varies From Design Point

677-3709
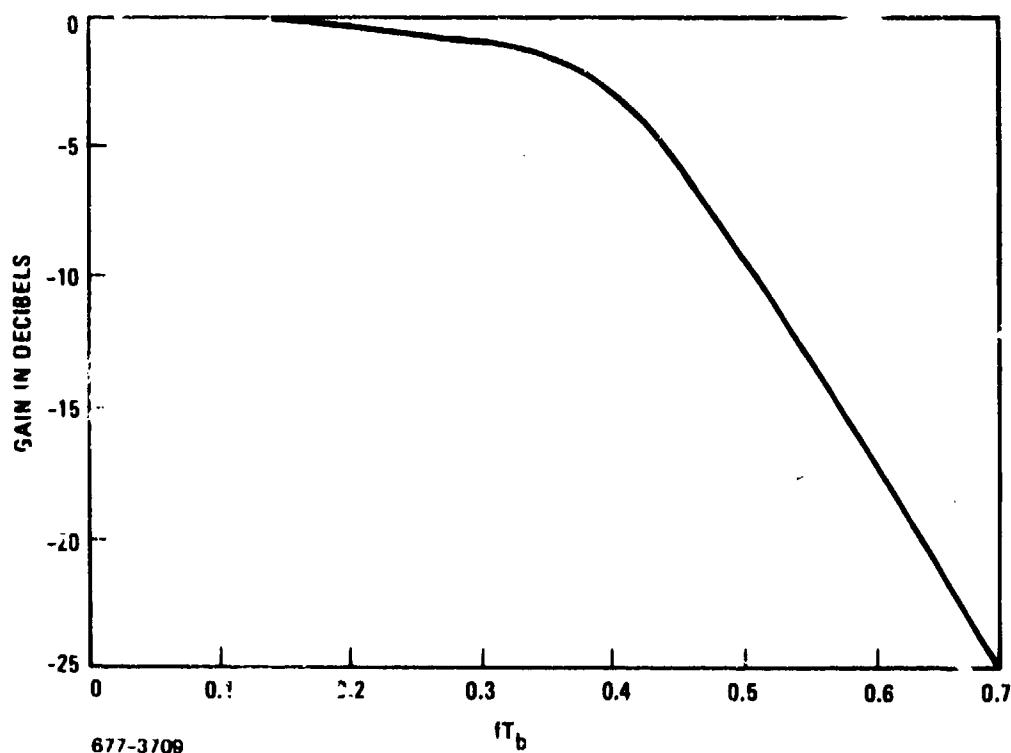
Figure 3-11. Amplitude Response of Linear Phase External Filter for Duobinary
Operation With Integrate-and-Dump Detector

PARAMETER = BT_b 0.3
= BANDWIDTH/BIT RATE
VITERBI ALGORITHM
DEMODULATION
ESTIMATED P_e

IDEAL
$\wedge$PSK

0.32

0.525

0.666

0.333

0.4

9775196
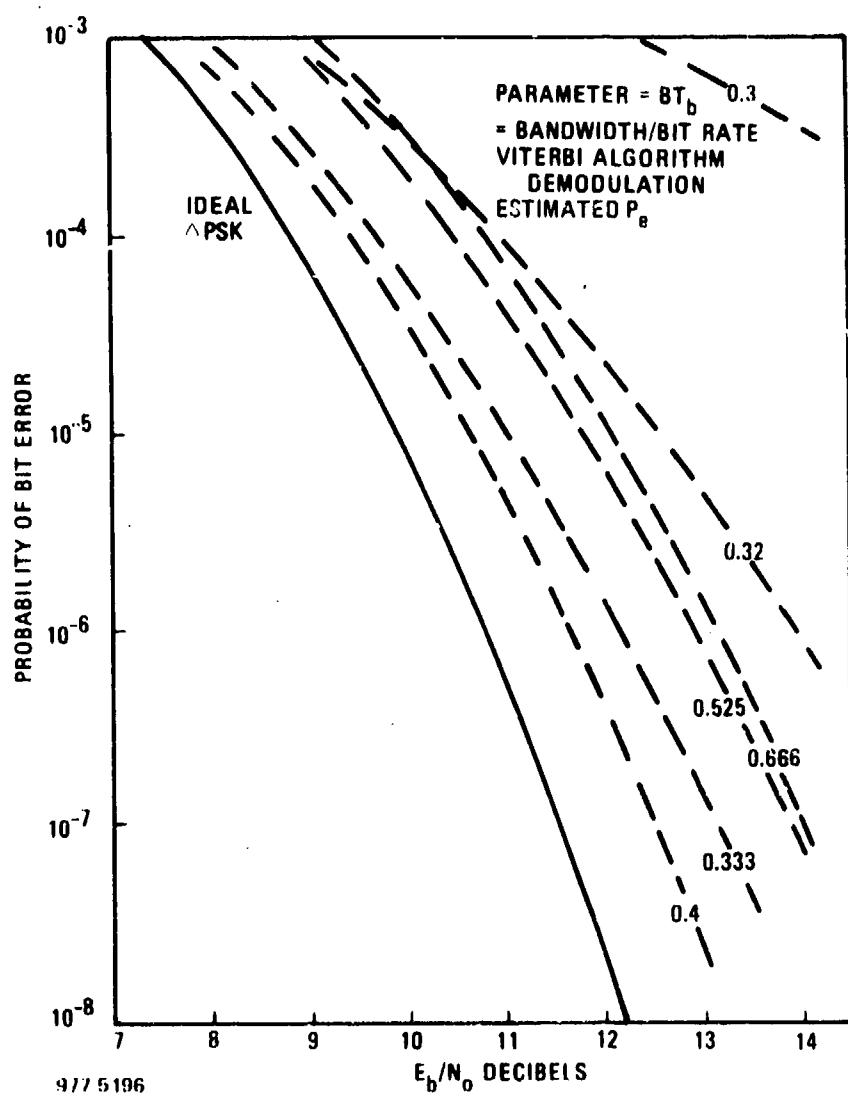
Figure 3-12. Duobinary SQPSK Performance With Linear-Phase, Maximally-Flat
External Filters and Integrate-and-Dump Detector

3.6 DUOBINARY PERFORMANCE WITH DECISION-DIRECTED CARRIER PHASE TRACKING

A decision-directed scheme to control gain and carrier phase for a SQPSK modem operating with duobinary demodulation has been described above. This section evaluates the degradation in bit error rate as the carrier tracking loop bandwidth is widened so that the phase error increases. A second-order loop is presumed in the computer simulation, iterated at the bit rate, and controlled by the decision-directed error, defined by (8) with quantizing according to (9). The gain control functions to drive the median amplitude of the data samples to unity, ignoring all amplitudes below 0.5. The bandwidth of this loop is approximately the same as the carrier phase tracking loop. Linear phase, maximally-flat filters (5-pole characteristic) are used in the transmitter and the receiver, since Figure 3-11 shows this gives an approximately optimum overall channel transfer function when the receiver has an integrate-and-dump detector.

Noting that the linear phase filters introduce no time delay, a clock tracking loop is unnecessary in the simulation since the optimum sampling time is known. In a practical sense, this is equivalent to having a very narrow clock tracking loop in an actual modem.

3.6.1 PERFORMANCE EVALUATION

Running the simulation at a specified E_b/N_o and carrier loop noise bandwidth B_L, the probability of error can be estimated. The degradation is the reduction in E_b/N_o to produce the same probability of error with ideal differentially-encoded conventional binary. Figure 3-13 plots the results, averaging over 12,800 bits. P_e is estimated for $E_b/N_o = 11$ dB and obtained by counting actual output errors at $E_b/N_o = 7$ dB. The carrier phase is initialized at zero error, and the gain is initialized at the value found from the simulations yielding Figure 3-5. The measured rms phase error at each B_L and E_b/N_o is marked on the curves in Figure 3-13.

The effect of carrier loop bandwidth is seen from Figure 3-13 to be small provided B_L/bit rate $<$ .005. Note that the degradation tends to increase at higher E_b/N_o, the reason being that intersymbol interference becomes more deleterious as the noise power is reduced.

2.0

DUOBINARY SQPSK
LINEAR PHASE, MAXIMALLY FLAT FILTERS
2ND ORDER CARRIER LOOP
DECISION–DIRECTED CONTROL
INTEGRATE-AND-DUMP

0.050 RAD

$E_b/N_0 = 11$ dB

0.030 RAD

0.020 RAD

0.081 RAD

$E_b/N_0 = 7$ dB

0.048 RAD

DEGRADATION IN DECIBELS

1.5

1.0

0.5

0

0   0.005   0.010   0.015   0.020

CARRIER TRACKING LOOP BANDWIDTH/TOTAL BIT RATE

677-3710
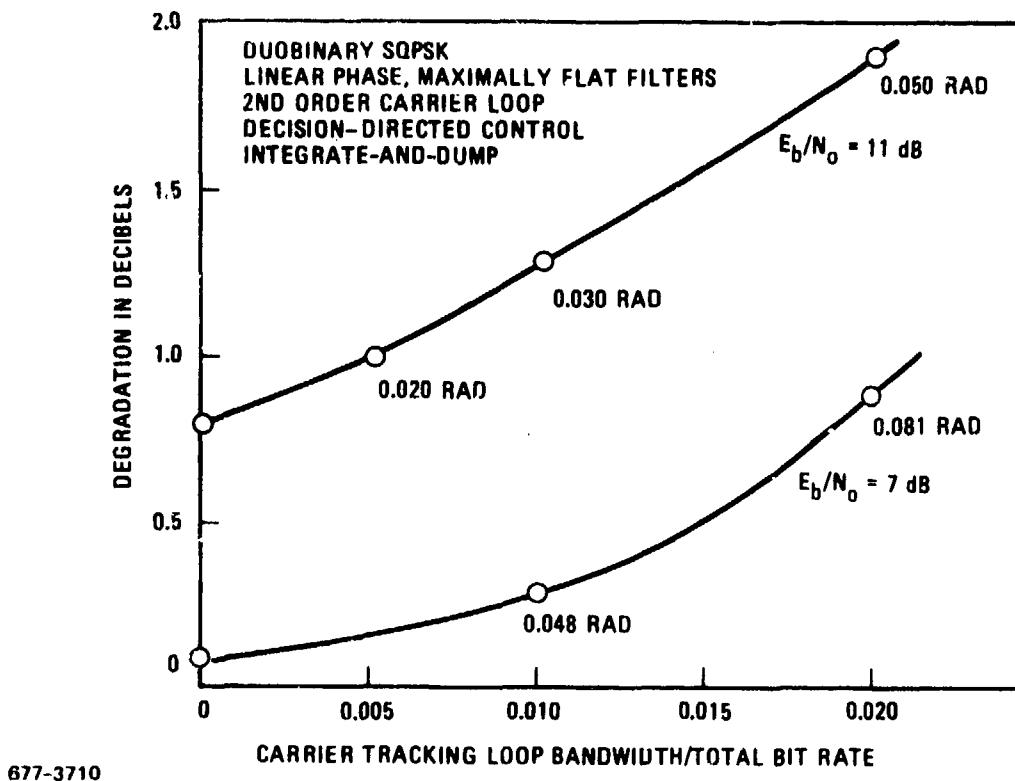
Figure 3–13. Duobinary SQPSK Degradation Due to Loop Tracking

3.6.2   DESIGN IMPLICATION

At a postulated minimum data rate of 100 Kbps for duobinary operation, the carrier loop bandwidth can be 500 Hz. The sweep rate $\dot{f}$ for acquiring an initial frequency uncertainty can be estimated from

$$\frac{2\pi\dot{f}}{(1.89\ B_L)^2} = .05 \tag{16}$$

where a tracking error of .05 radian is allowed in the second–order loop. Solving (16) for $B_L = 500$ Hz yields $\dot{f} = 7$ kHz/sec. For example, if the frequency uncertainty is ±25 kHz, the acquisition time is 7 seconds (time to sweep the total uncertainty of 50 kHz).

The simulation yielding Figure 3–13 also includes a sync detector based on the fraction of data amplitude samples falling within ± 0.2 of the ideal duobinary values (–1, 0, 1). The sync detector gives a positive indication even at $E_b/N_0 = 7$ dB and $B_L = .02$.

3-21

3.7 MODIFYING THE HARRIS MODEM MD-1002 FOR DUOBINARY OPERATION

The Harris modem MD-1002 is intended for SQPSK operation with conventional integrate-and-dump demodulation. Carrier phase tracking in this modem is via a quadrupling loop, where the 70 MHz IF output is quadrupled and phase locked to a reference, with a quadrature detector to detect acquisition of synchronization. There is a noncoherent AGC. The outputs of the I channel and Q channel product detectors control bit synchronization, and there is a coherent AGC prior to soft decision quantizing.

Appendix D discusses in detail the feasibility of modifying the Harris modem to SQPSK duobinary operation with external filters in the IF to produce the requisite duobinary transfer function for specified data rates. No modifications to the transmitter are necessary. In the receiver, the quadrupling loop for tracking carrier phase in conventional operation does not function properly when the duobinary response is formed. However, it appears feasible to drive the carrier VCO from the cross-product error voltage computed from the I and Q samples. Also, the bit synchronizer is modified to extract I and Q transition samples, which are treated as soft decisions for duobinary. A Viterbi algorithm is provided to process the duobinary soft decisions, and can interface similarly to an external decoder. Acquisition of synchronization is detected by the soft decisions tending to fall within the narrow sync zones centered on the ideal data amplitudes of -1, 0, 1 for duobinary. Figure 3-14 shows a block diagram of the duobinary SQPSK modem.

3.8 CONCLUSIONS

A decision-directed algorithm for carrier phase tracking can be derived for duobinary SQPSK operation to replace the quadrupling loop approach for conventional SQPSK. However, the delay-lock bit synchronizer can be retained. Simulation of combined carrier tracking and bit synchronization demonstrates the pull-in (acquisition) capability.

It is feasible to modify a SQPSK modem for duobinary operation using a set of fixed external filters to form the duobinary response. The modem retains the integrate-and-dump detector used for conventional binary. Accepting some degradation from ideal differentially encoded BPSK or QPSK, the data rate can be varied over an octave range from 1.5 bps/Hz to 3.0 bps/Hz, maintaining fixed external transmit and receive filters. The external filters are linear phase with a maximally-flat amplitude characteristic. Viterbi algorithm demodulation of duobinary is presumed in the receiver.
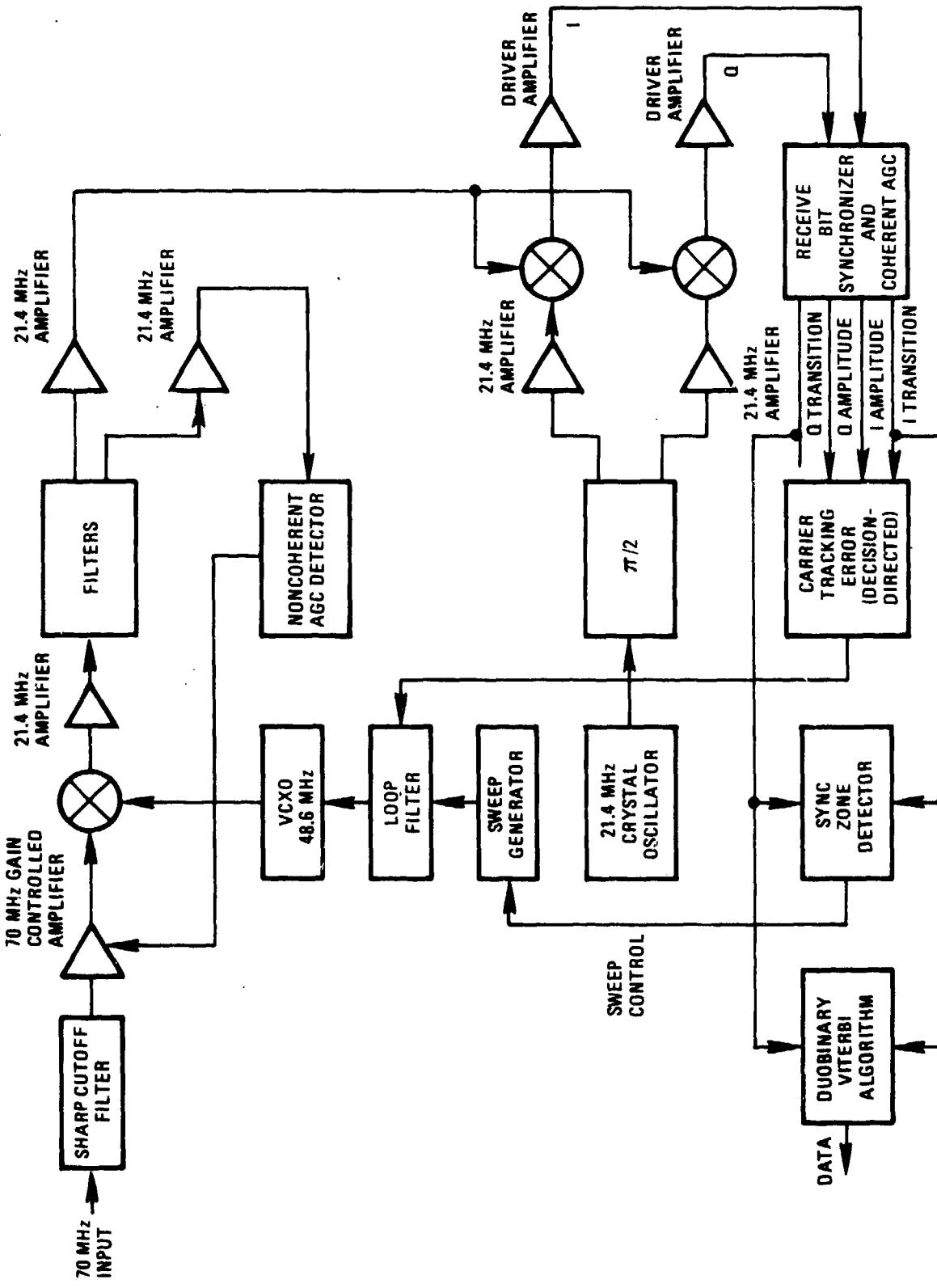
Figure 3-14. Block Diagram of Duobinary SQPSK Modem

977-5202

SECTION IV
ERROR CORRECTION CODING

This section studies the use of convolutional encoding/Viterbi decoding on the duobinary SQPSK channel. Error correction reduces the achievable data rate, hence degrades the bandwidth utilization, but has the advantage of conserving power because the required E_b/N_o is lower than for uncoded data at the typical assumed error rate of 10^{-5}. Since duobinary has the objective of increasing the data rate in a given bandwidth, hence is in conflict with the coding, the performance of the combined system must be studied carefully. Furthermore, with conventional SQPSK, an increased data rate with coding can alternatively be achieved by employing a code with less redundancy; i.e., a rate-3/4 code. Thus, a comparison between duobinary and conventional binary operation is appropriate.

4.1   IDEAL DUOBINARY CHANNEL AND ASSOCIATED METRIC

We begin by studying the ideal duobinary channel, which is defined as producing intersymbol interference from the present transmitted symbol. On any sample, this intersymbol interference has an amplitude equal to the amplitude contributed from the new symbol. Therefore, with binary modulation, a noise-free sample can take on one of the values −1, 0, 1, as illustrated in Figure 2-4. The associated metric for duobinary is given in Table 4-I, which applies independently to the inphase and quadrature components for QPSK or SQPSK. (Table 4-I is the same as Table 2-I, except for representing the transmitted symbols as binary 0, 1 instead of as positive or negative polarity.)

Table 4-I. **Metric for Duobinary Channel With Coding**

Present Symbol	New Symbol	Correct Sample Value	Metric Increment
0	0	1.0	v − .5
0	1	0.	0.
1	0	0.	0.
1	1	−1.0	−v − .5

4-1

For comparison, conventional binary ideally has no intersymbol interference, and the metric increment is +v or -v, depending on the hypothesized correct sample polarity.

In the absence of error correction coding, the transmitted symbol is derived from the data bit by differential encoding. Error correction introduces redundancy, and the coded symbols generated by the encoder occur at a rate exceeding the data rate. The redundancy of the code is defined in terms of a parameter equal to the data rate divided by the symbol rate. This parameter is called the code rate. Thus, a rate-1/2 code generates two symbols from one data bit, and a rate-3/4 code generates four symbols from three data bits.*

4.2   RATE-1/2 VITERBI DECODER FOR DUOBINARY CHANNEL

On a memoryless channel, such as ideal conventional binary, a rate-1/2 Viterbi decoder for a binary convolutional code of constraint length K has 2^{K-1} states. This is true because the metric increment is determined from the new coded symbol, which is a function of the last $K-1$ data bits and the new data bit. The state is defined by the last $K-1$ data bits.

With duobinary, which introduces memory into the channel, the metric increment is determined from both the present symbol and the new symbol. The present symbol is a function of the last K data bits, while the new symbol still is a function of the last $K-1$ data bits and the new data bit. Consequently, a rate-1/2 Viterbi decoder for a code of constraint length K must have 2^K states when designed for use in the duobinary channel. Compared to the standard Viterbi decoder for a memoryless channel, the number of states is doubled to handle the intersymbol interference of duobinary. With the aid of Table 4-I, the metric increment is determined for each possible state transition in the decoder. As usual, the Viterbi algorithm finds the sequence of states yielding the maximum metric. Note that the Viterbi decoder for duobinary is quite different from the standard rate-1/2 Viterbi decoder designed for the same code transmitted over the memoryless PSK channel.

To illustrate the Viterbi decoder for duobinary, let K = 5 so that the present symbol is a mod-2 sum of selected taps over the last 5 data bits.** Figure 4-1 shows an example of the state transitions, the present symbol and new symbol, and the resulting sample amplitude for duobinary. The metric increment for each state transition is found from Table 4-I.

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*Thus, code rate is a normalized parameter, in contrast to symbol rate or data rate.

**Note for simplicity, we illustrate just one set of taps producing the coded symbols. There are two independent sets for a rate-1/2 code.
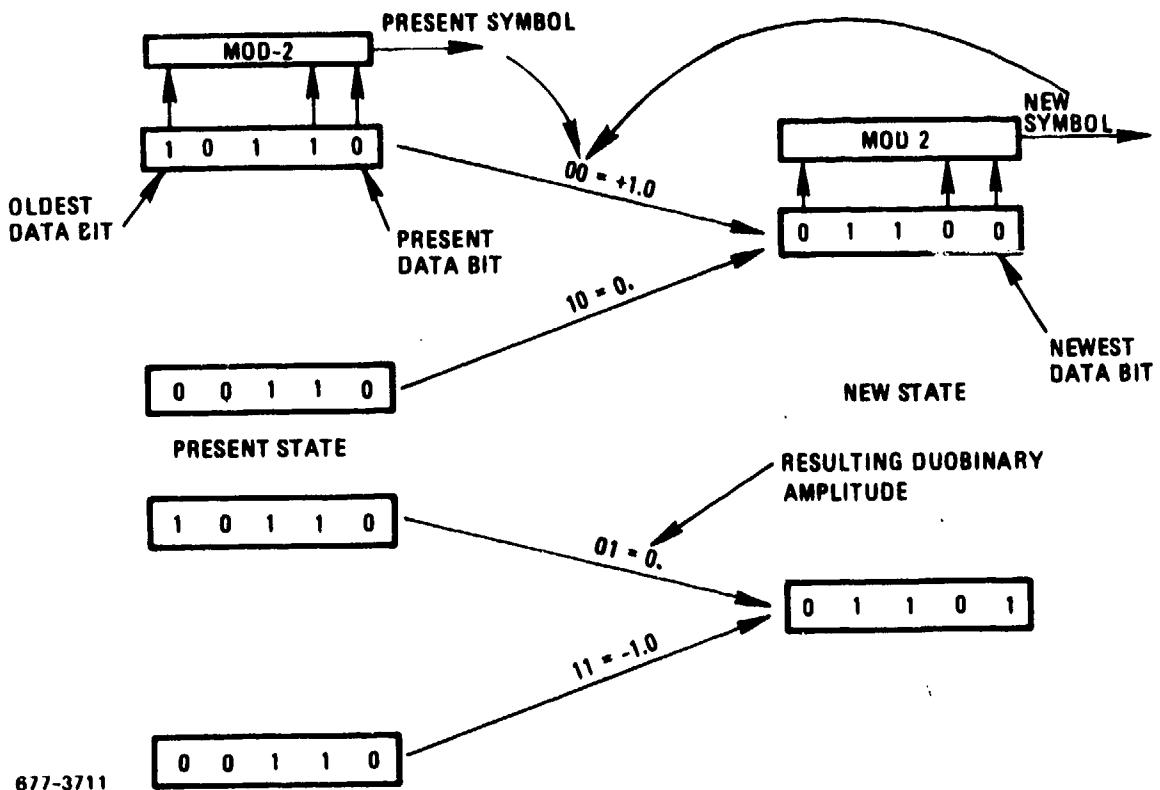
Figure 4-1. Illustration of State Transitions, Corresponding Present and New Symbols, and Resulting Duobinary Amplitude

Cataloguing all possible state transitions and the corresponding metric increments into a stored table, the Viterbi decoder for duobinary can be simulated. As suggested by Figure 4-1, for a rate-1/2 code, the present states are grouped in pairs differing in the oldest data bit, and the new states are grouped in pairs differing in the newest data bit.

The present study of a rate-1/2 convolutional code for the duobinary channel assumes the respective coded symbols from the pair of independent mod-2 sums are transmitted on independent inphase and quadrature components of QPSK. In this model, there is no intersymbol interference between the independent coded symbol streams. Duobinary creates intersymbol interference only between the present symbol and the new symbol on each independent stream.

4.2.1 COMPUTER SIMULATION OF RATE-1/2 CODE ON IDEAL DUOBINARY CHANNEL

A simulation was carried out assuming a QPSK channel with ideal duobinary response. The sampling rate is equal to the coded symbol rate. Table 4-I defines the sample amplitude resulting from the present and new coded symbols transmitted over the channel.

4-3

To begin, there is no error correcting code, and the Viterbi algorithm has only two states (i.e., $K = 1$). Simulation results for transmitting random data are plotted in Figure 4-2 and closely approach the ideal differentially encoded PSK curve.* These results are similar to Figure 2-11, for a simulation of a SQPSK narrowband channel adaptively equalized to approximate the duobinary response. The error rate is measured by counting erroneous data bits output from the Viterbi algorithm at the specified E_b/N_o. Differential encoding of the data bits is presumed.**
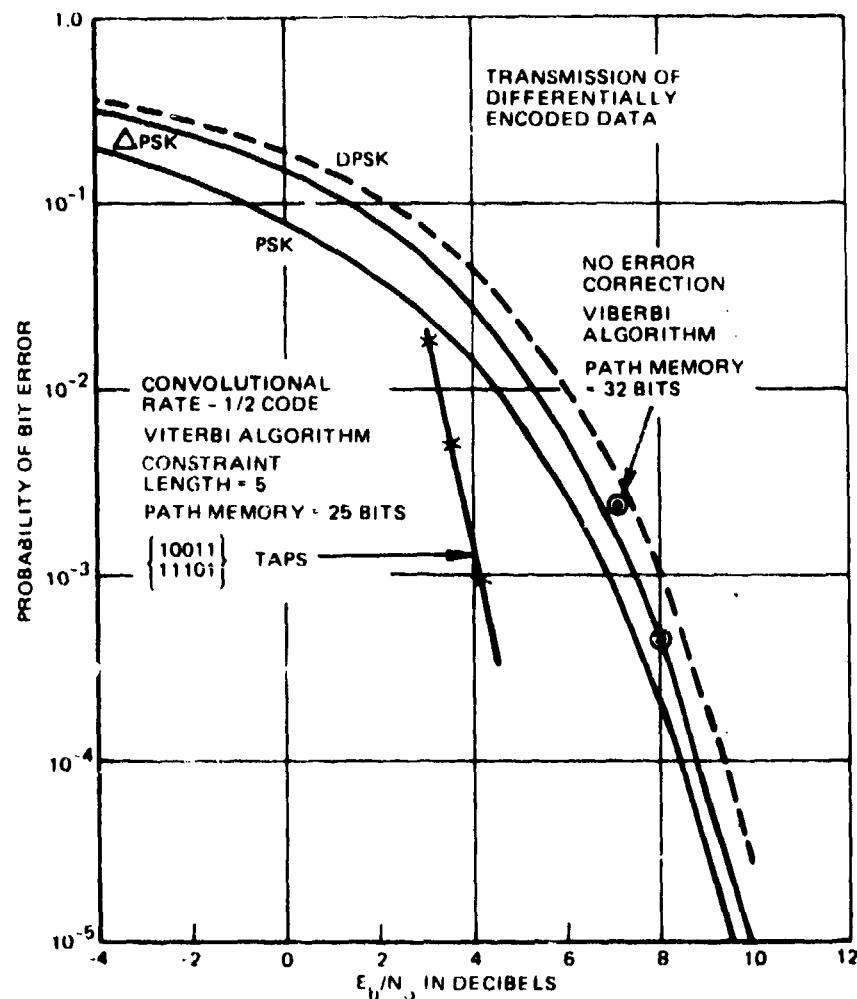
776-3594
UNCLASSIFIED

Figure 4-2. Performance on Ideal Duobinary Channel

*E_b/N_o is defined with respect to average power at the receiver. For amplitudes -1, 0, 1 of duobinary, the average power is 0.5.

**Differentially encoded data and a transparent convolutional code is an easy way to accommodate 180° phase ambiguity of BPSK. QPSK has 90° ambiguity also, and this must be resolved by distinguishing the inphase and the quadrature components.

Next, a rate-1/2 convolutional code of constraint length 5 is employed. The selected code is the same as found optimum for the memoryless conventional binary channel. (Section 4.2.3 shows this to be a good code for the duobinary channel also.) The code is defined by the two sets of taps for the mod-2 sums, as listed in Figure 4-2. Error rate results with differentially encoded data are plotted in Figure 4-2. These results are observed to be only slightly worse (by roughly 0.5 dB) than previously found in the Phase A Final Report for the same convolutional code and a Viterbi decoder on the conventional binary channel.

4.2.2   MOST LIKELY ERROR FOR DUOBINARY

Section 4.2.1 demonstrated that a rate-1/2 convolutional code optimized for the memoryless binary channel also works well when applied to the duobinary QPSK channel. The question remains whether improved performance on the duobinary channel could be obtained from a different code. To help answer this question, the most likely error in decoding on the duobinary channel needs first to be identified; then, the prospects for improvement can be assessed.

A rate-1/2 convolutional code generates a pair of symbols as a function of each new data bit and the encoder state specified by the K-1 previous data bits, where K denotes the constraint length. For QPSK, one symbol is transmitted on I, and the second symbol is transmitted on Q. Convolutional encoding and transmission on the ideal QPSK duobinary channel is modelled as shown in Figure 4-3. The delay of one bit of the intersymbol interference of ideal duobinary causes the present symbol to be added to the new symbol, in parallel on I and Q, and a ternary output results on each.

776-3579
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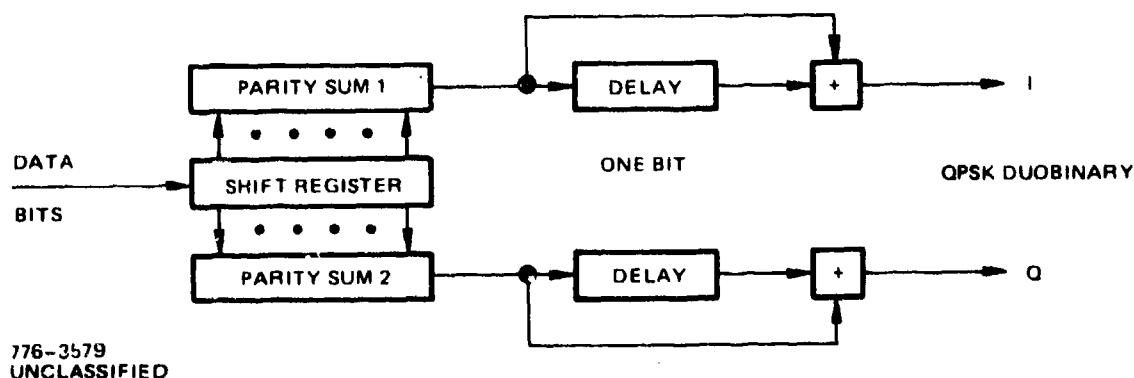
Figure 4-3.   Model of Ideal Duobinary QPSK Channel With Rate-1/2 Coding

4-5

Figure 4-4 shows an example of a random sequence and its conversion to a ternary waveform as a consequence of the duobinary response. The duobinary has zero amplitude when the symbol sequence has a transition, and positive or negative amplitude when the sequence does not switch. Figure 4-4 has been drawn with the duobinary timing offset to emphasize that the binary channel is converted to duobinary when the sampling is displaced by half the symbol duration.

(A)   BIT SEQUENCE

776-3287
(UNCLASSIFIED)

(B)   DUOBINARY WAVEFORM
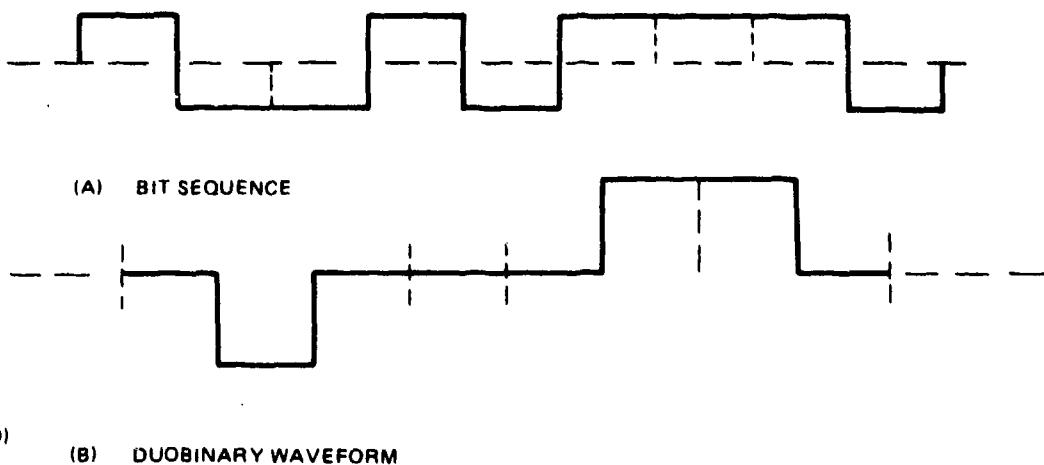
Figure 4-4.   Bit Sequence and Corresponding Duobinary

The probability of error in distinguishing two different sequences of transmitted bits on the coherent duobinary channel is now studied. The energy in the difference between the waveforms is the significant parameter when optimum demodulation is performed assuming additive white Gaussian noise in the receiver. Figure 4-5 shows an example of two sequences differing by one bit, and the resulting difference between the duobinary waveforms.

If the conventional binary waveform has unit power, the binary amplitude levels are ± 1. The difference between the two sequences has amplitude 2 or -2 for the single bit duration where the bit is changed; hence, the energy in the difference waveform is 4. If the duobinary waveform has unit power, the ternary amplitude levels are $\pm\sqrt{2}$ and 0. The difference between the two duobinary waveforms has amplitude $\sqrt{2}$ or $-\sqrt{2}$ for two bit durations; hence, the energy is 4 also.

4-6

+1.0
-1.0
(A)   BIT SEQUENCE

(B)   BIT SEQUENCE (ONE BIT IS CHANGED)

(C)   DIFFERENCE BETWEEN BINARY WAVEFORMS

$+\sqrt{2}$
0
$-\sqrt{2}$
(D)   DUOBINARY

(E)   DUOBINARY (ONE BIT IS CHANGED)

677-3712   (F)   DIFFERENCE BETWEEN DUOBINARY WAVEFORMS
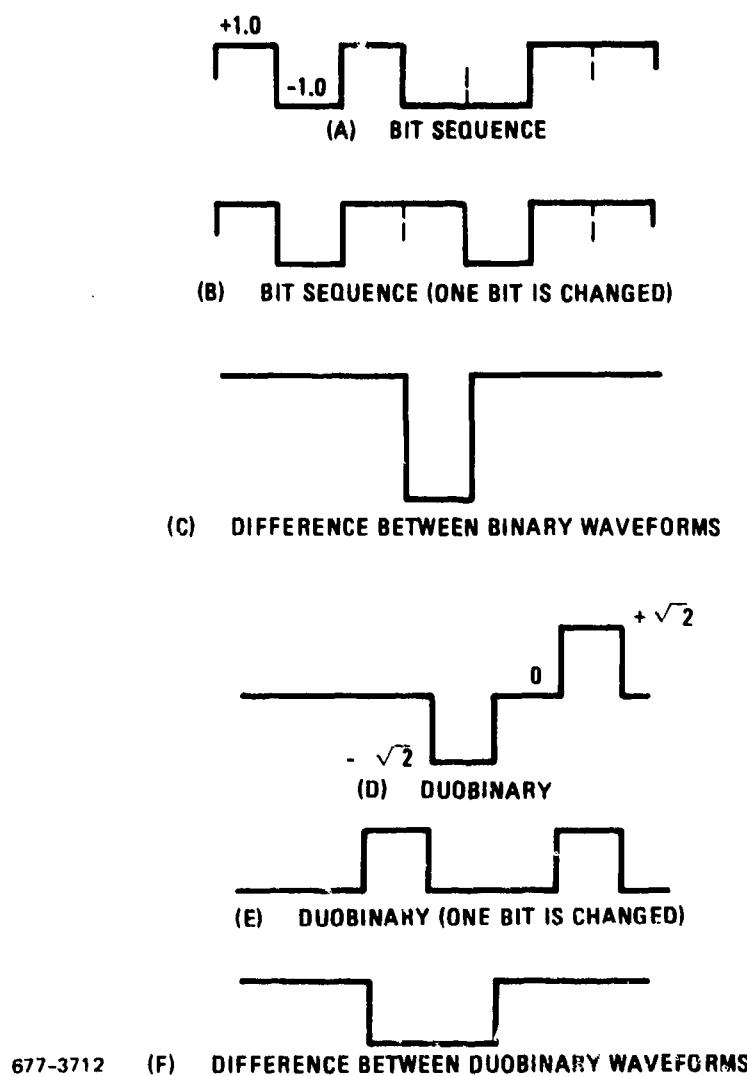
Figure 4-5. Mechanism of Error With Duobinary

With a maximum-likelihood demodulation process, duobinary asymptotically has the same error probability as binary, at the same average power and assuming white noise in the receiver. The Viterbi algorithm is an implementation of maximum-likelihood demodulation. Actually duobinary has a somewhat higher error rate than binary because an incorrect waveform can have more than one bit changed, yet the energy in the difference is still 4.

Suboptimum demodulation of duobinary utilizes only the receiver waveform over a single bit duration, and there is an asymptotic penalty of 3 dB, since the distance between adjacent amplitude levels is $\sqrt{2}$ for duobinary compared with 2 for conventional binary.

4-7

The error mechanism can be characterized even more directly by making use of a property of duobinary, that it is a form of differential encoding of the bit sequence. That is, a transition in the bit sequence produces zero amplitude, while no transition gives full amplitude (positive or negative depending on the prior bits). Suboptimum demodulation of duobinary which maps the ternary decision for each bit into a binary output is based on this observation. One way to ensure a discernible difference between the duobinary waveforms corresponding to different bit sequences is now evident; one sequence should be made to have transitions where the second does not, and vice versa. Of course, for some pairs of sequences, one duobinary waveform can be positive where the second is negative, and this yields an even greater waveform difference, if this property can be exploited.

An artificial example can be given where the 3 dB improvement from maximum-likelihood demodulation of duobinary is not realized. Postulate an alternating bit sequence, which yields a zero amplitude duobinary waveform. If the alternating bit sequence is complemented after some point, the duobinary waveform has a single nonzero amplitude, and the energy in the difference waveform is half the normal value. Figure 4-6 illustrates this artificial case. Note that when the alternations in the bit sequence cease, the missing energy in the difference waveform finally occurs. Therefore, the maximum-likelihood demodulation process for duobinary requires sufficient path memory storage (i.e., decoding delay) that the probability of having the artificial case is sufficiently low. With random data, the probability of getting 20 alternating bits is 10^{-5}; hence, the delay should certainly exceed 20 bits for the typical probabilities of error of interest.

4.2.3 OPTIMIZATION OF RATE-1/2 CONVOLUTIONAL CODE FOR DUOBINARY

Applying the above principle for ensuring a difference between duobinary waveforms, we can find the optimum rate-1/2 convolutional code for QPSK duobinary operation. Comparing any pair of code words to evaluate the probability of error, we wish to maximize the total number of transitions which occur in the symbols of one word but not of the other. (Note, a word consists of two parallel symbol streams as shown in Figure 4-3.)

Now, observe that the transitions in a code word correspond to 1's in the differentially decoded code word. Since a unit shift of any code word still is a code word and differential decoding is mod-2 addition of the word with a unit delay of itself, the differentially decoded code word must be itself a code word.

(A)   BIT SEQUENCE (ALTERNATING BITS)

(B)   BIT SEQUENCE COMPLEMENTED AT BIT NO. 4

(C)   DUOBINARY COR .ESPONDING TO (A)

776-3289   (D)   DUOBINARY CORRESPONDING TO (B)
(UNCLASSIFIED)
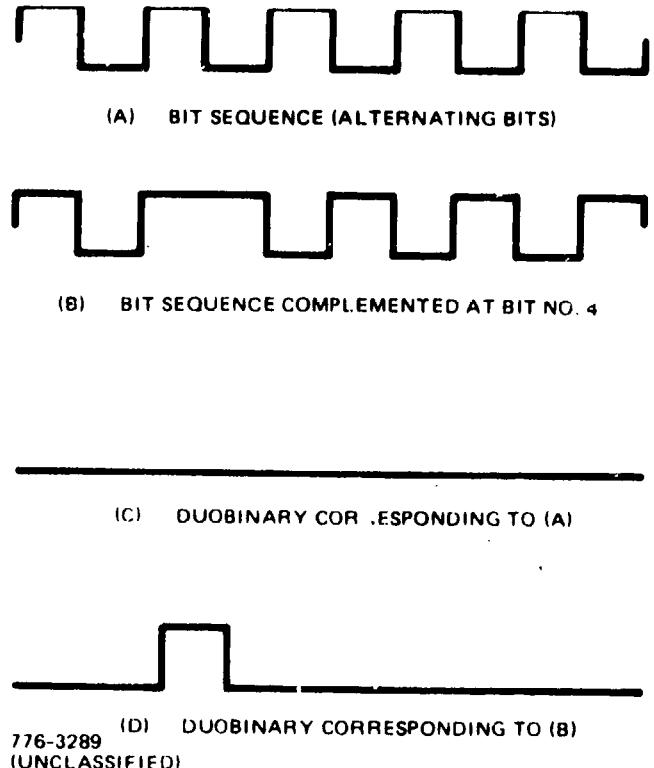
Figure 4-6.   Artificial Case Where Improvemer⁴ From Maximum Likelihood
Demodulation of Duobinary is not . alized

Requiring that one code word have as many 1's as possible where the
second code word does not, and vice versa, is equivalent to requiring that the
mod-2 sum of the two code words have as many as 1's as possible. But, again, this
mod-2 sum yields a code word. Thus, the final conclusion is that the optimum
rate-1/2 convolutional code for QPSK duobinary should maximize the minimum weight
of any code word; i.e., should maximize the free distance.

The, perhaps surprising, result is that the same rate-1/2 convolutional
code which is optimized for the conventional binary channel by maximizing the free
distance is also optimum for the QPSK duobinary channel in the sense of maximizing
the number of non-simultaneous transitions.

A transparent code contains the all 1's code word, hence, a word
with continual transitions. This code word produces zero amplitude after
the duobinary response. Comparing this code word with any other,
the minimum energy (in appropriate units) in the waveform difference is obviously
equal to the free distance of the code. However, it is possible that the minimum

energy in the waveform difference may exceed the free distance for a non-transparent code, since the zero-amplitude waveform cannot occur. Then, over the duobinary channel, a non-transparent code would be superior to a transparent code with the same free distance. (Of course, synchronization is more difficult with the non-transparent code because a 180° phase shift in the receiver cannot be ignored.)

4.2.4 COMPUTATION OF MINIMUM METRIC DIFFERENCE

The rate-1/2 Viterbi decoder for the duobinary channel can be utilized to find the minimum metric difference, which by the argument above is proportional to the energy in the difference between the correct waveform and the most closely matching incorrect waveform. The metric increments used in the decoder are given in Table 4-I, and the constant of proportionality is 0.5 with signal amplitudes of -1, 0, 1. (This corresponds to an average power of 0.5.)

For a constraint length 5 code, which is non-transparent and has free distance equal to 7, the minimum metric difference, adjusted to assume unit power in the signal for a random data bit sequence, is found to be 8. The theory above claims a lower bound of 7. (This is the free distance multiplied by the constant of proportionality.)

For a constraint length 7 code, which is transparent and had a free distance equal to 10, the minimum metric difference is found to be 10.

Thus, the conjecture that on the duobinary channel, a non-transparent code should be better than a transparent code of the same free distance appears to be true.

4.2.5 ASYMPTOTIC VERSUS ACTUAL CODING GAIN

The code word comparison with the minimum metric difference dominates probability of error asymptotically as E_b/N_o grows large. For equal powers in a duobinary signal and in a conventional binary signal, and using the same rate-1/2 convolutional code, the minimum metric difference for conventional binary is twice that for duobinary. Thus, as E_b/N_o becomes large, duobinary is asymptotically inferior by 3 dB, for the same code.

The minimum metric difference occurs infrequently, however, with a random data bit sequence over the duobinary channel, and most metric differences are higher; possibly even exceeding that for conventional binary. At a probability of error typically of interest, say 10^{-5}, the E_b/N_o difference with coding between duobinary and conventional binary should be considerably less than 3 dB. This is borne out by simulation results in Figure 4-2.

4.3   RATE-3/4 VITERBI DECODER FOR DUOBINARY CHANNEL

The Phase A Final Report described a technique for converting a rate-1/2 convolutional code to a rate-3/4 code by a repetitive pattern of deleting two out of every six symbols generated by the rate-1/2 encoder. This technique is advantageous for the memoryless conventional binary channel because it enables the rate-3/4 code to be decoded as a rate-1/2 code using a standard rate-1/2 Viterbi decoder. The deleted symbols are restored to the rate-1/2 decoder as zero-amplitude erasures, and the internal states and metric increments within the rate-1/2 decoder therefore do not have to be modified. *

The Phase A Final Report found the optimum rate-3/4 code derivable from a rate-1/2 code of constraint length 7. (Optimum means to maximize the free distance of the code.) Figure 4-7 describes the encoder for this optimum rate-3/4 code, which has free distance = 6. Figure 4-8 is intended to show in detail how the symbols from the rate-1/2 encoder are deleted to produce rate-3/4, and how they are arranged for transmission over the QPSK or SQPSK channel. Six symbols, numbered 1 to 6, are generated by the rate-1/2 encoder from a block of three successive data bits, and the first and third are deleted as depicted. This deletion process repeats to generate a block of four coded symbols from each successive block of three data bits. The symbols are transmitted in sequence alternately on I and then on Q, for the QPSK or SQPSK channel.

FREE DISTANCE = 6
ASYMPTOTIC CODING GAIN = 6.5 dB
CONSTRAINT LENGTH = 7
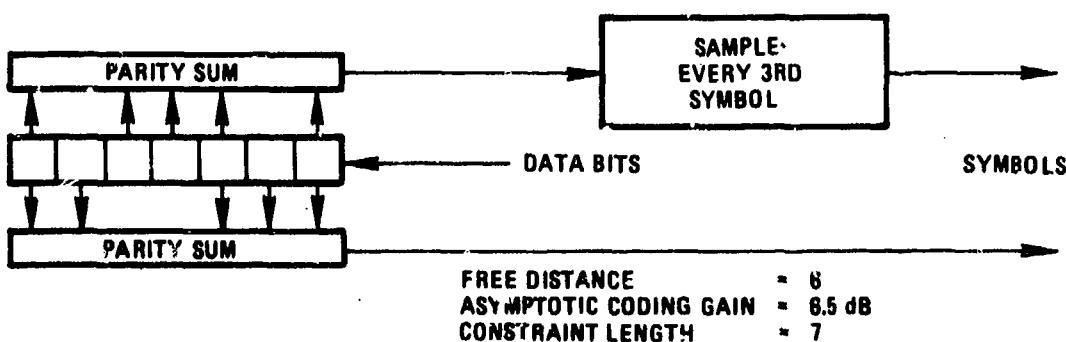
677-3713

Figure 4-7. Optimum Rate-3/4 Convolutional Code

---

*As presently designed, the Linkabit KY-801 cannot be utilized as a rate-3/4 decoder in this manner without some internal modifications because the 3-bit input quantization to the decoder does not include a zero amplitude input level. The metric increments corresponding to the allowed input levels to the KY-801 are +4, +3, +2, +1, -1, -2, -3, -4. The internal modifications are to allow a metric increment of 0, corresponding to an erasure. Also, results in Appendix C suggest such rate-3/4 utilization benefits from longer path memories.

```
FIRST PARITY      1  3  5  1  3  5  1  3  5

SECOND PARITY     2  4  6  2  4  6  2  4  6

(A)   ORIGINAL SEQUENCE OF
      SYMBOLS FROM RATE-1/2 ENCODER

FIRST PARITY      x  x  5  x  x  5  x  x  5

SECOND PARITY     2  4  6  2  4  6  2  4  6

(B)   PATTERN OF DELETIONS TO GIVE RATE-3/4

I                    2  5  2  5  2  5

Q                    4  6  4  6  4  6

(C)   TRANSMISSION OF RATE-3/4 CODE ON QPSK CHANNEL
```

677-3714

Figure 4-8. Sequence of Symbols for Optimum Rate-3/4 Code

Alternatively, the optimum rate-1/2 code of constraint length 7 can be converted to rate-3/4 by the pattern of deletions which maximizes the free distance for that code. Figure 4-9 shows the encoder for this, and Figure 4-10 gives the resulting sequence of symbols for QPSK or SQPSK, where the first and fourth symbols are deleted from the six symbols generated from a block of three successive data bits. Although the free distance of this rate-3/4 code = 5, while the optimum code has free distance = 6, performance on the memoryless conventional binary channel is essentially identical to that of the optimum code, for typical error rates of interest. *

Over the duobinary QPSK or SQPSK channel, the significance of Figure 4-8 or 4-10 is that because of the deletions, the decoder for rate-3/4 decoding must provide a state structure which extends over an additional data bit than for rate-1/2 decoding. For example, in Figure 4-8, symbol 5 on the I channel is immediately

*The reason is that the number of incorrect words of minimum distance 6 in the optimum rate-3/4 code is much larger than the number of incorrect words of distance 5 in the other code.

677-3715
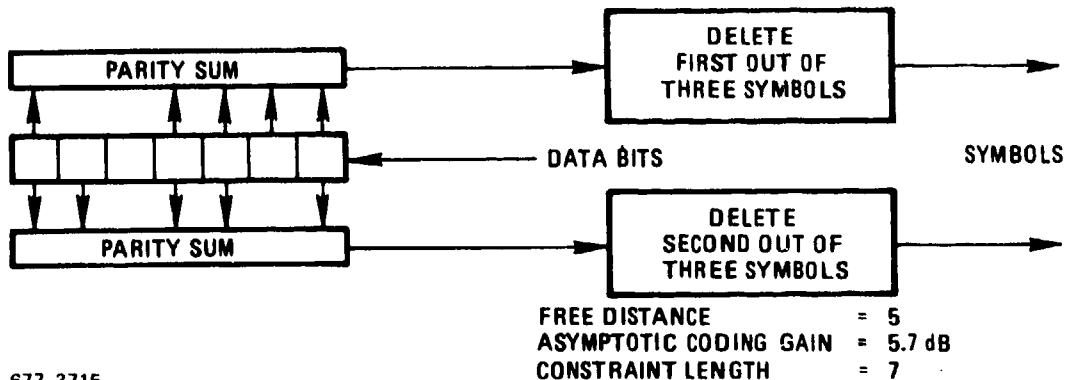
Figure 4-9. Rate-3/4 Convolutional Code Derived From Optimum Rate-1/2 Code

```
FIRST PARITY      1  3  5  1  3  5  1  3  5
SECOND PARITY     2  4  6  2  4  6  2  4  6
    (A)   ORIGINAL SEQUENCE OF SYMBOLS FROM RATE-1/2 ENCODER
FIRST PARITY      X  3  5  X  3  5  X  3  5
SECOND PARITY     2  X  6  2  X  6  2  X  6
    (B)   PATTERN OF DELETIONS TO GIVE RATE-3/4
I                    2  5  2  5  2  5
Q                    3  6  3  6  3  6
    (C)   TRANSMISSION OF RATE-3/4 CODE ON QPSK CHANNEL
```

677-3716

Figure 4-10. Sequence of Symbols for Rate-3/4 Code Derived From Optimum
Rate-1/2 Code

preceded by symbol 2, which was actually generated 2 data bits previously. Conse-
quently, for a rate-3/4 code derived from a rate-1/2 code of constraint length
K, the number of decoder states must be 2^{K+1}, or four times the number in the
standard Viterbi decoder for the rate-1/2 code. As an additional complication, the
immediately previous symbol has a different relative position in the original sequence
for each of the four symbols transmitted; hence, the metric increment table is
different for each of the three data bits corresponding to a block of four symbols. In
contrast, for the rate-1/2 decoder designed for the duobinary QPSK channel, the
metric increment table is the same for each data bit.

4-13

It is judged that the Viterbi decoder for a rate-3/4 convolutional code transmitted over the duobinary QPSK channel is very complex, compared to a standard rate-1/2 decoder for the same constraint length. Such complexity is tolerable only if significant performance benefits are attained.

4.4   SIMULATION OF CODED SQPSK SYSTEM PERFORMANCE

This section evaluates the performance of a coded duobinary SQPSK system and makes comparison to a coded conventional SQPSK system. The objective of duobinary is to increase the attainable symbol rate in a given bandwidth, hence, the data rate for a fixed code rate. The same objective is reached by the alternative of using a higher rate code with conventional binary transmission.

The computer simulation model described in Appendix A for SQPSK in a channel adaptively equalized for duobinary demodulation was modified to include the rate-1/2 or rate-3/4 convolutional code/Viterbi decoder. Because of anticipated difficulties in decision-directed equalization for duobinary at low E_b/N_o, the adaptive equalization control was derived from the correct symbols, rather than being decision directed. (The error for the LMS algorithm is defined with respect to the correct sample amplitude given in Table 4-I as a function of the present and the new coded symbols.) The Viterbi decoder is designed for an ideal duobinary QPSK channel; i.e., it uses the metric increments specified in Table 4-I.

The transmit and receive filters are 5-pole Butterworth, and either a sampling detector or an integrate-and-dump detector can be used in the receiver The simulation proceeds by first equalizing to form the least mean square approximation to the desired duobinary response. The Viterbi decoder assumes that a perfect duobinary response has been realized. After convergence, the equalizer tap weights and the bit sampling time are frozen, and the Viterbi decoder is activated. The white Gaussian noise is added to the transmitted signal prior to the receive filter. The transmitted signal is periodic, represented by 16 samples per symbol. There are 64 symbols transmitted in one period on both the inphase and the quadrature components; hence, 64 data bits for a rate-1/2 code and 96 data bits for a rate-3/4 code in one period. The noise is treated as periodic in the receive filter; however, new noise samples are generated for each successive period. The error rate is obtained either by directly counting errors in the decoder's output or by the estimation technique for the Viterbi algorithm described in Appendix C. The data is differentially encoded prior to being convolutionally encoded.

4.4.1   COMPARISON BETWEEN RATE-1/2 AND RATE-3/4 CODING FOR DUOBINARY OPERATION

Since the Viterbi decoder for a rate-3/4 code over the duobinary SQPSK channel is significantly more complex than the decoder for a rate-1/2 code over the same channel, a performance comparison between rate-3/4 and rate-1/2 coding is appropriate. A constraint length 5 code is assumed for both, as given in Figure 4-11. This comparison for equal constraint lengths is actually unfair to rate-1/2 operation, since, compared to the rate-1/2 decoder for duobinary, the rate-3/4 decoder for duobinary stores double the number of states and, furthermore, has a different metric increment table for each of the three data bits generating a block of four coded symbols. Results are plotted in Figure 4-12.

With uncoded duobinary SQPSK, included in Figure 4-12 also, the data rate cannot exceed 3 bps/Hz without significant degradation, as shown by the two points plotted. This result means the channel can no longer be equalized to a good approximation of the ideal duobinary response when the transmitted symbol rate exceeds 3 bps/Hz. With rate-1/2 coding, this corresponds to a data rate of 1.5 bps/Hz. With rate-3/4 coding, this means a data rate of 2.25 bps/Hz.
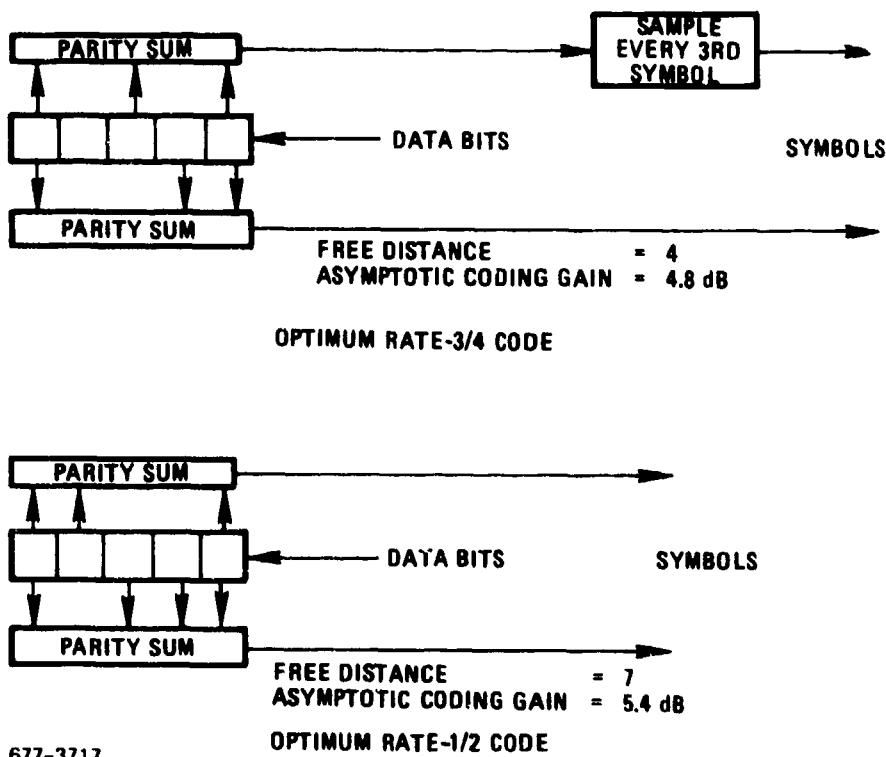
Figure 4-11. Optimum Constraint Length 5 Codes
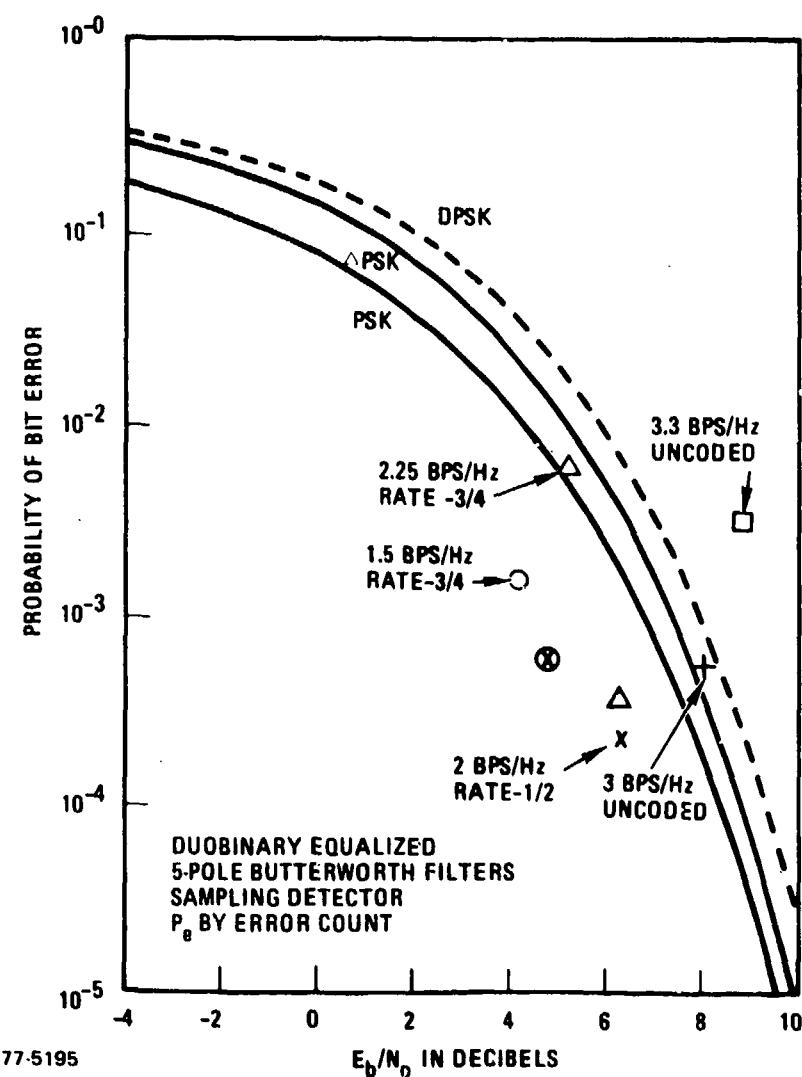
Figure 4-12. Duobinary SQPSK, Coded and Uncoded

It is found that rate-1/2 coding has sufficient redundancy to tolerate poor equalization at a high transmitted symbol rate. Figure 4-12 plots error rate with rate-1/2 coding for a data rate of both 1.5 bps/Hz and 2 bps/Hz. Performance is essentially identical at the two rates, even though the symbol rate for the latter is 4 bps/Hz, for which uncoded performance would be unacceptable. However, performance with rate-1/2 coding degrades rapidly when the data rate exceeds 2 bps/Hz.

Figure 4-12 also plots error rate results for rate-3/4 coding at a data rate of 2.25 bps/Hz. Performance is found to degrade rapidly when the data rate exceeds 2.25 bps/Hz. The required E_b/N_o for rate-3/4 coding at 2.25 bps/Hz is higher than for rate-1/2 at 2 bps/Hz.

It is concluded that rate-3/4 coding for the duobinary SQPSK channel has essentially no advantage over rate-1/2 coding for this channel, since the achievable bandwidth utilization is not significantly better and a higher E_b/N_o is necessary. Furthermore, the rate-3/4 Viterbi decoder for duobinary is much more complex than the rate-1/2 decoder for duobinary. Therefore, rate-3/4 coding for the duobinary SQPSK channel is dropped from further consideration.

4.4.2 RATE-1/2 CODING FOR DUOBINARY SQPSK, VARYING DATA RATE IN FIXED FILTER

This section assumes the same duobinary SQPSK channel simulation, except for the introduction of rate-1/2 convolutional encoding/Viterbi decoding, as derived in Section 3.5.4 for uncoded data. The transmitter and receiver each have a zero-phase, maximally-flat filter, with a 5-pole cutoff characteristic. The receiver includes an integrate-and-dump detector matched to the symbol duration T_b. This channel approximates the desired duobinary response at the design point $BT_b = .4$. If the data rate is varied in a fixed bandwidth, the integrate-and-dump detector is stretched proportionally.

The receiver tracks carrier phase and gain generally as described in Section 3. Specifically, a single complex tap weight is controlled by the decision-directed LMS algorithm, according to (5). Because there is no phase shift in the filters, the receive bit timing is known; however, it actually is tracked in the simulation by the delay-lock bit synchronizer.

Rate-1/2 coded duobinary SQPSK performance is evaluated as a function of the ratio of channel bandwidth to data rate; the objective being to assess the effect of varying the data rate transmitted through fixed bandwidth filters. The probability of error of the rate-1/2 Viterbi decoder for duobinary is estimated by the technique discussed in Appendix C. The optimum rate-1/2 code of constraint length 7 is utilized. This code is defined by the convolutional encoder in Figure 4-9 (without the deletions indicated in Figure 4-9 to give rate-3/4). The simulation results are presented in Figure 4-13. In similarity with the uncoded case, Figure 3-12, the required E_b/N_o is minimized at $BT_b = 0.4$, which corresponds to data transmission at 1.25 bps/Hz. When the data rate is reduced in the fixed bandwidth filters, the duobinary performance degrades due to excessive noise, despite the presence of an integrate-and-dump detector matched to the longer bit duration. When the data rate is increased, the performance again degrades due to the effect of intersymbol interference. However, in contrast to the uncoded case where performance degraded
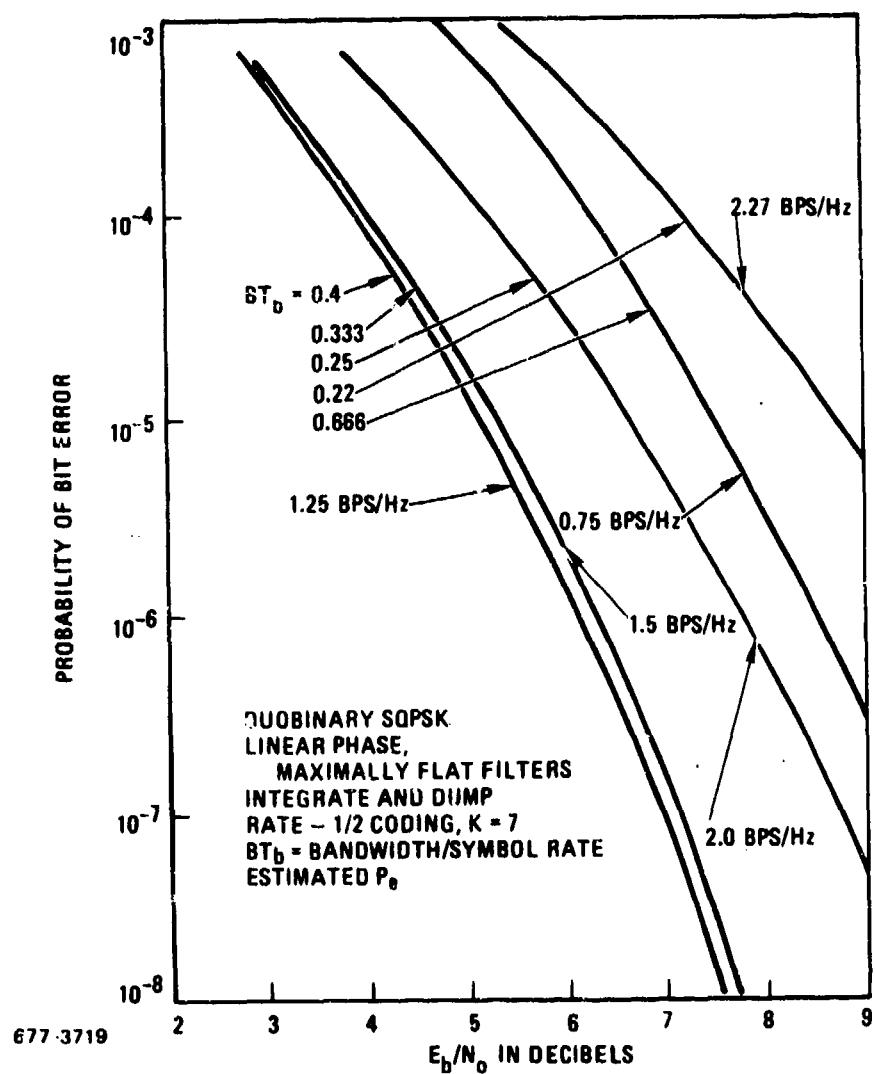
Figure 4-13. Rate-1/2 Coded Duobinary SQPSK With Linear-Phase, Maximally-Flat Filters

rapidly when $BT_b < .33$, with rate-1/2 coding, BT_b can easily be as low as .23. Thus, a data rate of 2 bps/Hz can easily be achieved at low E_b/N_o with rate-1/2 coded duobinary SQPSK (such that the coded symbol rate is 4 bps/Hz).

Note that the 3 dB point on the maximally-flat external filter is selected as defining channel bandwidth. There is a filter in both the transmitter and the receiver, and E_b/N_o is defined for the signal power at the output of the transmit filter.

4.4.3   SQPSK CONVENTIONAL SIMULATION RESULTS (RATE-3/4)

For conventional SQPSK, the external channel filters have zero phase and the amplitude characteristic plotted in Figure 4-14, which was derived in the Phase A Final Report. Identical filters are used in the transmitter and the receiver. The definition of bandwidth is taken from the 3 dB point on the originally maximally-flat characteristic; however, after equalization, the defined bandwidth corresponds to the 2 dB point relative to the peak response. (Thus, the 3 dB bandwidth relative to the peak response is slightly wider.) In the application to coding, bit rate in Figure 4-14 refers to the coded symbol rate.

776-3973
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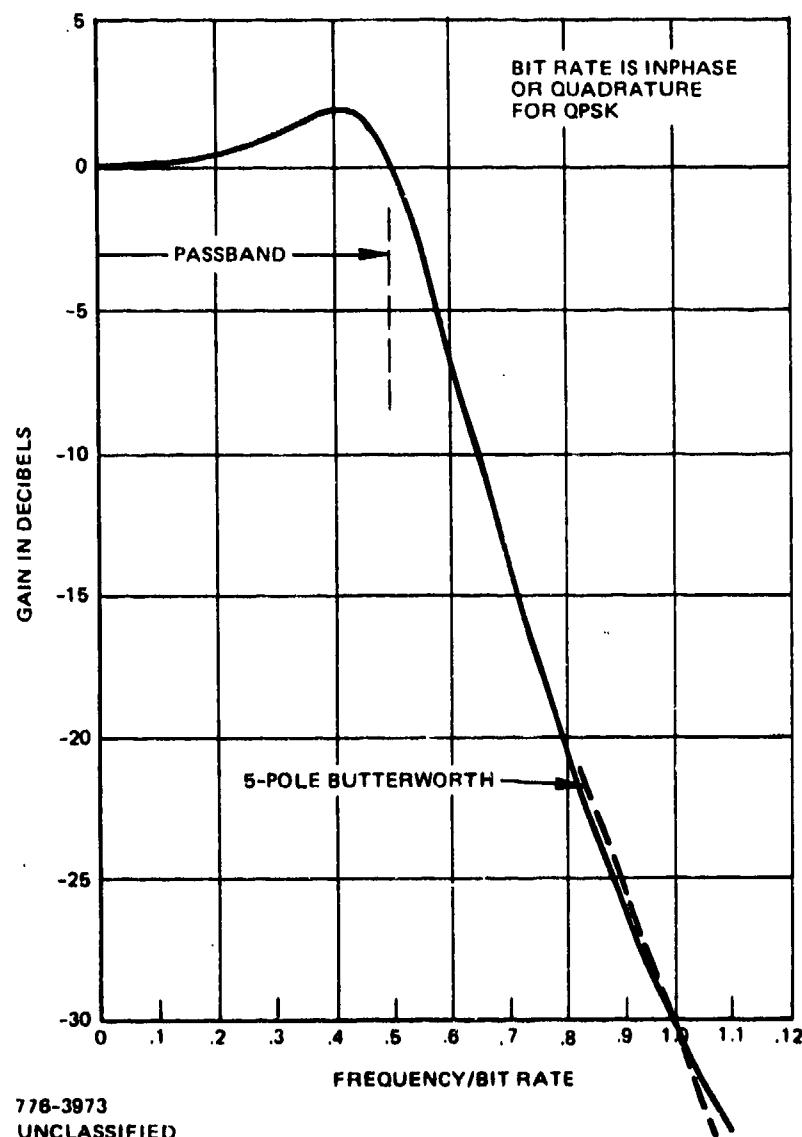
Figure 4-14.   Equalized Filter for Transmitter and Receiver of Conventional
SQPSK

With rate-3/4 coding over the conventional SQPSK channel, the Viterbi decoder is the same design as the rate-1/2 decoder for the memoryless conventional binary channel. The rate-1/2 code of constraint length 7 is converted to the optimum rate-3/4 code by deletions, as shown in Figure 4-7. Figure 4-15 presents the estimated performance. As the data rate is reduced, the performance improves; i.e., in contrast to the uncoded case as described by Figure 7-4 of the Phase A Final Report, there does not appear to be a "bump" for $.5 < BT_b < 1.0$.

677-3720
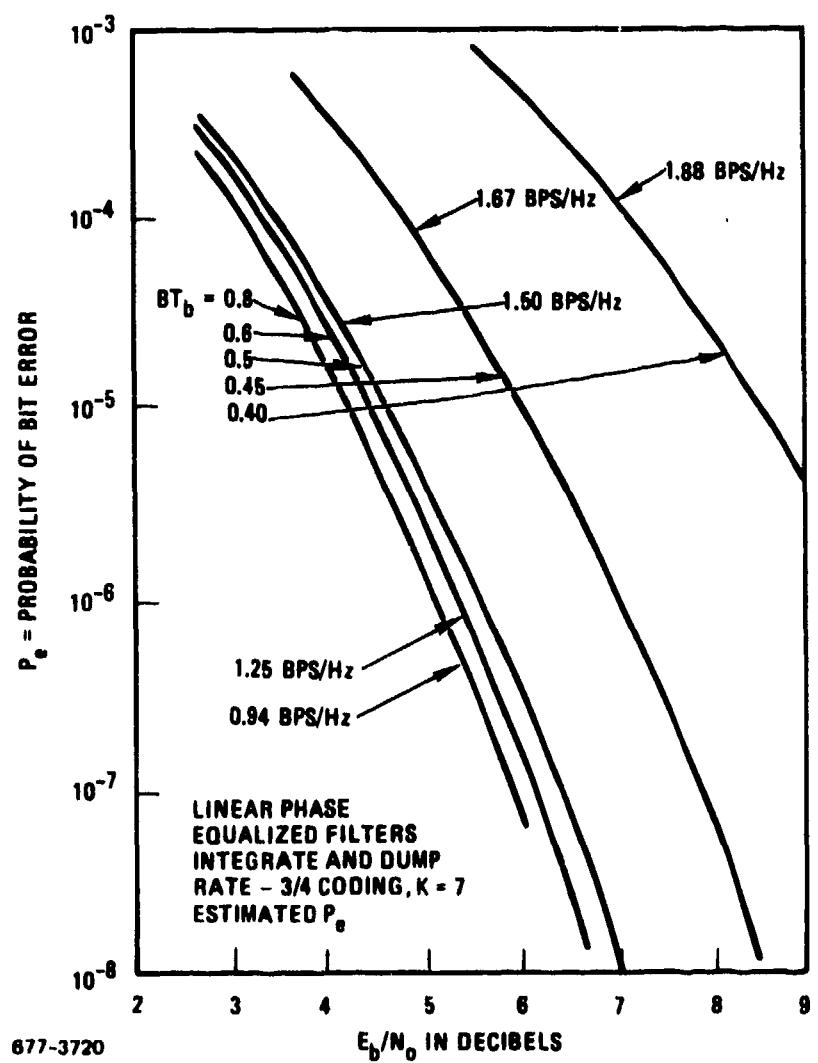
Figure 4-15. Rate-3/4 Coded Conventional SQPSK With Linear Phase Equalized Filters

Appendix E discusses some possible system modifications to enable the Harris MD-1002 modem to operate with external rate-3/4 convolutional encoding/Viterbi decoding. Clock conversion poses perhaps the most difficult interface problem.

4.4.4 COMPARISON OF DUOBINARY AND CONVENTIONAL BINARY

A significant advantage of conventional SQPSK is that the rate-1/2 Viterbi decoder for the memoryless binary conventional channel already exists in the DSCS and could be converted relatively easily to rate-3/4 operation, while the rate-1/2 Viterbi decoder for duobinary SQPSK is a new design. Furthermore, comparison of Figures 4-13 and 4-15 shows that rate-3/4 conventional binary is better than rate-1/2 duobinary for data rates up to approximately 1.6 bps/Hz, and the coding gain is substantial (approximately 5 dB reduction in E_b/N_o at 10^{-5} error rate). At data rates beyond 1.6 bps/Hz, performance in the conventional binary channel rapidly degrades.

In the range of data rates from 1.6 bps/Hz up to 2 bps/Hz, rate-1/2 duobinary offers some coding gain. However, comparing Figure 4-13 with uncoded conventional SQPSK at 2 bps/Hz, Figure 7-4 of the Phase A Final Report, the reduction in E_b/N_o at 10^{-5} error rate is only approximately 3 dB. Thus, in the range of data rates where rate-1/2 coded duobinary can operate while rate-3/4 coded conventional cannot, the achievable coding gain is relatively modest. Since the rate-1/2 Viterbi decoder for the duobinary channel is quite different from a conventional rate-1/2 Viterbi decoder, the performance benefit does not appear to justify the necessary financial investment.

4.5 CONCLUSIONS

Rate-1/2 coding over the conventional SQPSK channel can achieve a bandwidth utilization of 1.1 bps/Hz as may be seen from results of the Phase A study. Rate-3/4 coding over the conventional SQPSK channel can achieve up to 1.6 bps/Hz, and the E_b/N_o is perhaps 1 dB higher than for rate-1/2. Furthermore, the rate-3/4 Viterbi decoder is a straightforward modification of the standard rate-1/2 decoder. Uncoded conventional SQPSK can operate at 2 bps/Hz. Bandwidth utilization beyond 2 bps/Hz can be attained by uncoded duobinary SQPSK, up to a limit of approximately 3 bps/Hz.

In the range 1.6 bps/Hz up to 2.3 bps/Hz, rate-1/2 coded duobinary SQPSK offers the possibility of a modest coding gain (reduction in required E_b/N_o). However, the financial investment in the requisite Viterbi decoders, of an entirely new design, does not appear to be justified by this performance gain.

SECTION V
SINGLE ACCESS (TDMA) DUOBINARY PERFORMANCE

This section examines the performance and bandwidth requirements for single-access service (or TDMA) using duobinary SQPSK signalling. The effects of filter characteristics, phase distortion, and saturating amplifiers are determined for several channel configurations. Throughout, an emphasis is placed on maximizing bandwidth utilization.

The results of Section III show that the use of phase distortionless maximally-flat filters in the transmitter and receiver produce near-optimal performance (in conjunction with integrate-and-dump detection). This section further evaluates the single-access duobinary performance as a function of the filter bandpass both with and without the inclusion of an adaptive equalizer in the receiver. Transmission at 3 bps/Hz of bandwidth is shown to be feasible in the quasilinear channel.

Use of a hard-limiting transmitter for TDMA is found to eliminate the need for power control of the accesses. In such severe saturating channels, transmission of duobinary SQPSK at 2.5 bps/Hz is possible.

The various system elements are as described in Sections II and III and modelled as described in Appendix A. The channel configuration varies, and a block diagram of the appropriate channel model is given for each simulation.

5.1   FILTER PHASE DISTORT: SIMULATION RESULTS

All degradations are determined for an $E_b/N_o = 10$ dB at the receiver input. Error rates are computed using the estimation technique described in Appendix C. System degradation is evaluated by first determining that receiver input E_b/N_o which would produce the same resulting probability of bit error in an ideal ΔPSK system, converting this E_b/N_o to decibels, and subtracting this number from the actual receiver input $E_b/N_o = 10$ dB. Since Section IV concludes that error correction coding is not attractive for use with duobinary, no degradations are given for low E_b/N_o. Figure 5-1 shows the system simulated for single-access duobinary signalling, but no AM-PM conversion exists in the current simulation.
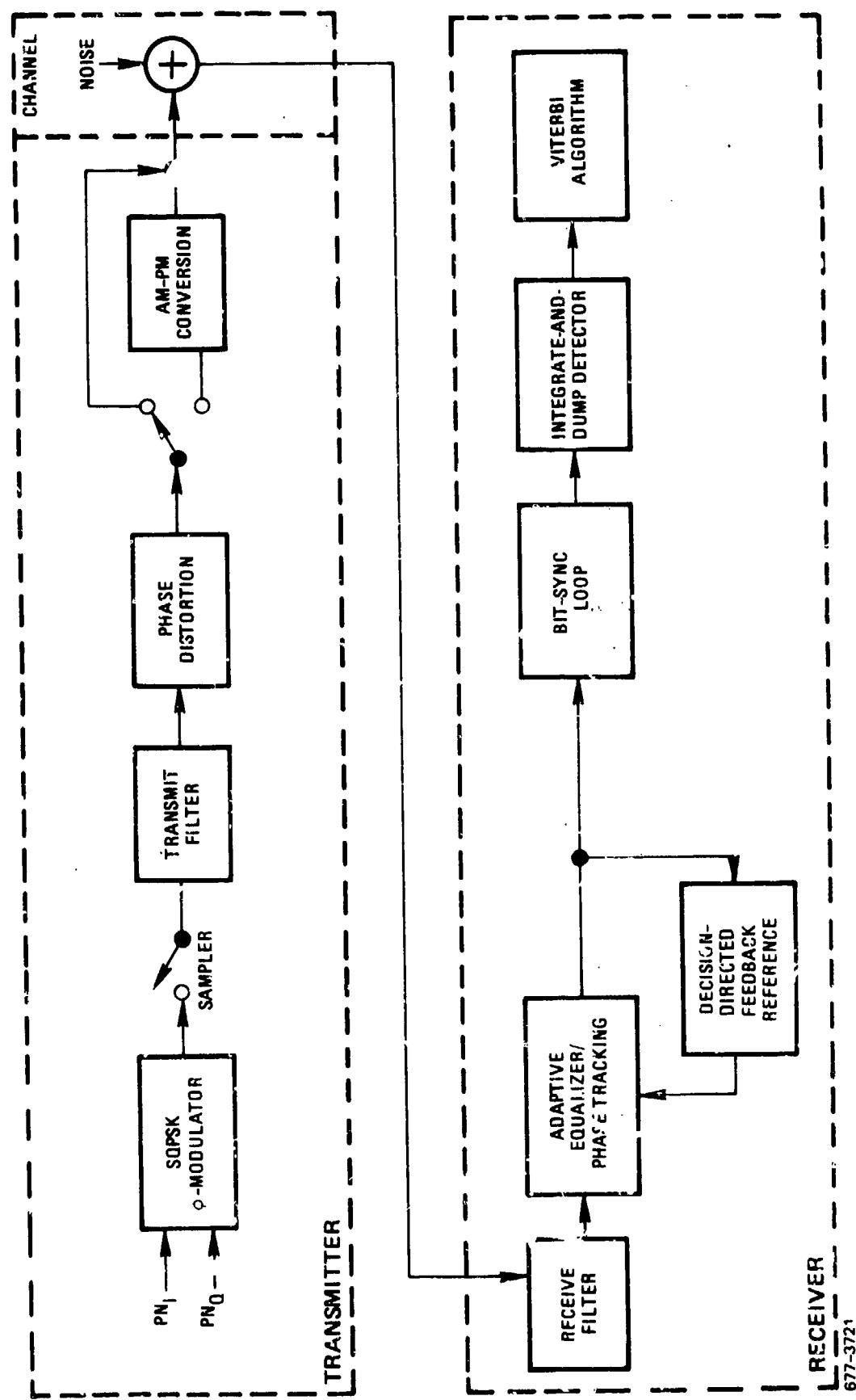
Figure 5-1. Duobinary System Modelled

677-3721

5-2

Curves are run with and without the use of an adaptive equalizer in the receiver. If an equalizer is used, the reference signal is developed through use of decision-directed feedback as described in Section 2.2. Eight (complex) taps are used with tap spacing equal to the bit rate. If no equalizer is used, AGC and decision-directed phase tracking are accomplished by use of the algorithm given in Section 3.1 for controlling a single complex tap weight. An integrate-and-dump detector is used in all cases.

5.1.1 FILTER EFFECTS

Five-pole zero-phase maximally-flat filters are used in the transmitter and receiver. Figure 5-2 gives the degradation as a function of filter (one-sided) bandwidth/bit rate ratio (BT_b) for a linear channel with no phase distortion. As shown, the minimum degradation occurs for $BT_b = 0.4$, increasing for BT_b greater or less than this value. Degradation increases very rapidly for $BT_b < 0.333$. As $BT_b \to \infty$, the degradation approaches 3 dB, as predicted in Section 3.5.1. With SQPSK, $BT_b = .333$ corresponds to transmission at 3 bps/Hz of bandwidth while $BT_b = .4$ implies 2.5 bps/Hz of bandwidth. Figure 5-2 exhibits performance similar to that given in Figure 3-10 where the filter was equalized at the design point and then the data rate was varied.
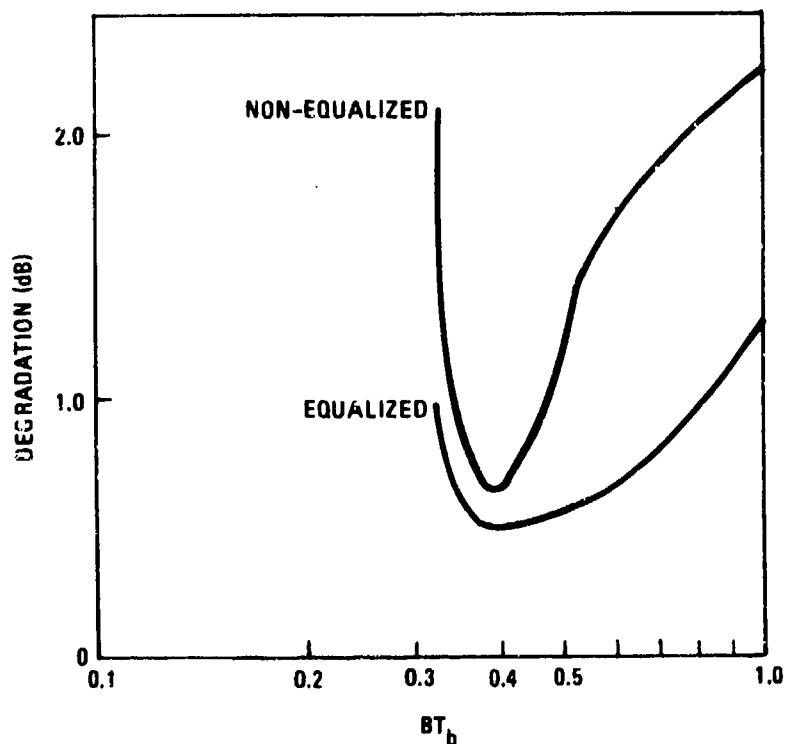
677-3722

Figure 5-2. Degradation Versus BT_b of Maximally-Flat Filters at $E_b/N_o = 10$ dB

5-3

Figure 5-2 also gives the resulting degradation as a function of filter bandwidth when an adaptive equalizer is used in the receiver. The equalizer has 8 taps with tap spacing equal to T_b. As shown, use of an equalizer lowers the degradation for all BT_b and minimal degradation occurs for a broader range of BT_b surrounding $BT_b = .39$. Degradation remains under 1 dB from $BT_b = .32$ to $BT_b = .8$.

5.1.2 EFFECTS OF PHASE DISTORTION

Phase distortion arises from several sources, including filters, converters, and ant nnas. The resulting degradation depends on the magnitude and form of the phase distortion. This section investigates the degradation in a SQPSK duobinary system resulting from sinusoidal, cosinusoidal, and parabolic phase distortion as a function of the peak error. Two major results are shown. First, degradation is not only dependent on the peak phase error but is a function of the type of phase distortion present, the system bandwidth, and the ripple frequency (for sinusoidal and cosinusoidal distortion). In addition, duobinary channels are more sensitive to phase distortions than SQPSK channels. The effects of the various forms of phase distortion are analyzed below, followed by simulation results.

5.1.2.1 Sinusoidal Phase Distortion

The sinusoidal phase distortion of period T_R is given by

$$\theta(\omega) = \beta \sin(\omega T_R) \tag{17}$$

where T_R determines the ripple period in the frequency domain and the phase varies between $\pm\beta$. If T_R equals the bit duration T_b, there is one ripple cycle in the first null bandwidth $[0 \le \omega \le 2\pi T_b^{-1}]$. Ripple frequency $FR = T_R^{-1}$.

If $s(t)$ is the signal waveform with Fourier transform $S(\omega)$, the time domain response after distortion is

$$r(t) \quad \frac{1}{2\pi} \int_{-\infty}^{\infty} S(\omega) e^{j(\omega t + \beta \sin\omega T_R)} d\omega$$

$$\sum_{k=-\infty}^{\infty} J_k(\beta) s(t + k T_R) \tag{18}$$

Therefore, paired echos are produced by sinusoidal distortion. For small β, only the $k = \pm 1$ terms contribute significant intersymbol interference. In addition,

the echos are antisymmetric. Because sinusoidal distortion produces a complex symmetric transfer function, duobinary BPSK and QPSK are identically degraded in a channel without saturation or AM-PM conversion, and there is no cross-channel interference.

5.1.2.2 Cosinusoidal Phase Distortion

Cosinusoidal phase distortion of period T_R and amplitude β is given by

$$\theta(\omega) = \beta \cos(\omega T_R) \tag{19}$$

For small β, the resulting time response is

$$r(t) \approx J_0(\beta) s(t) + j [J_1(\beta) s(t - T_R) + J_1(\beta) s(t + T_R)] \tag{20}$$

where the intersymbol interference is in quadrature with the pulse. Therefore, the two duobinary QPSK channels interact, with the degradation being similar to that produced by sinusoidal distortion. For duobinary BPSK, however, the intersymbol interference is in phase quadrature and has no effect on the demodulation unless it affects tracking loops due to the resulting phase steps produced by bit transitions. Note that if $T_R = T_b$, the bit duration, the intersymbol interference falls directly on adjacent pulses.

5.1.2.3 Parabolic Phase Distortion

The assumed parabolic phase characteristic is

$$\theta = \beta \left[\frac{\omega T_R}{2\pi}\right]^2 \tag{21}$$

where β is the phase error developed at (radian) frequency $\omega = 2\pi/T_R$. This phase variation yields the time delay variation

$$\frac{d\theta}{d\omega} = \beta \frac{T_R^2}{2\pi^2} \omega \tag{22}$$

The response to a data pulse with parabolic distortion is similar to that produced by cosinusoidal distortion since the transfer function is nonsymmetrical. For this reason, the duobinary QPSK channels interact to product degradation greater than that for BPSK.

5.1.2.4 Simulation Results

Figures 5-3 through 5-6 give the degradation due to sinusoidal, cosinusoidal, and parabolic distortion for a receiver with and without an adaptive equalizer. Figures 5-3 and 5-4 use filters with $BT_b = .333$ while Figures 5-5 and 5-6 use filters with $BT_b = .4$. Figures 5-3 and 5-5 assume the ripple frequency $FR = 1.$, while Figures 5-4 and 5-6 were run with $FR = .333$. For $BT_b = .333$, $FR = .333$ implies one (sinusoidal or cosinusoidal) phase ripple over the one-sided 3 dB filter bandwidth. Similarly, for the case of parabolic phase distortion, the peak phase error (SK) is reached at the 3 dB filter bandwidth. For filters with $BT_b = .4$, 1.2 ripples occur over the filter bandwidth for sinusoidal or cosinusoidal phase distortion while the peak parabolic phase error is increased by 40 percent at the filter 3 dB point.
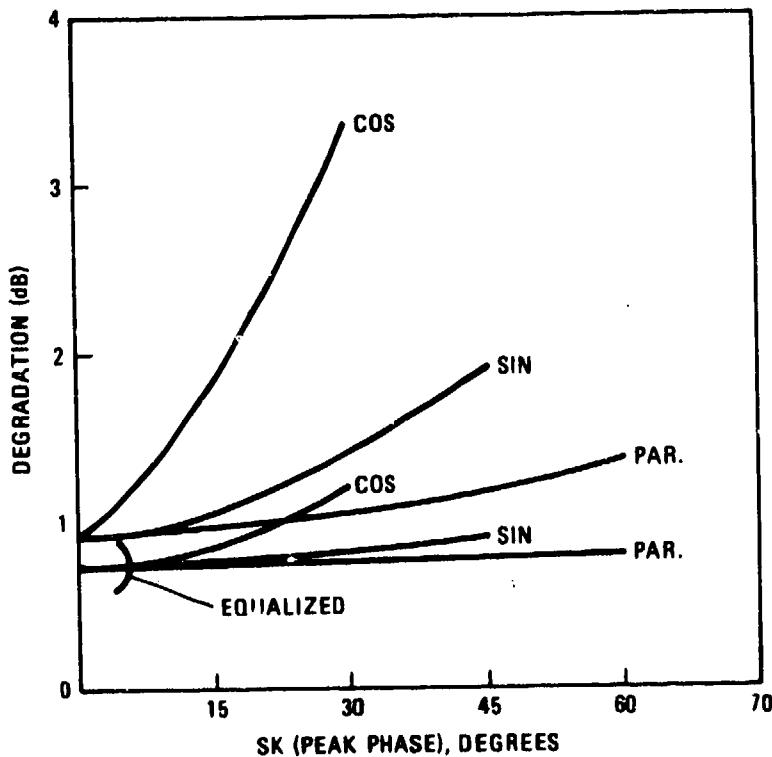
677-3723

Figure 5-3. Degradation Due to Phase Distortion ($BT_b = .333$, $FR = 1.$)
$E_b/N_o = 10$ dB
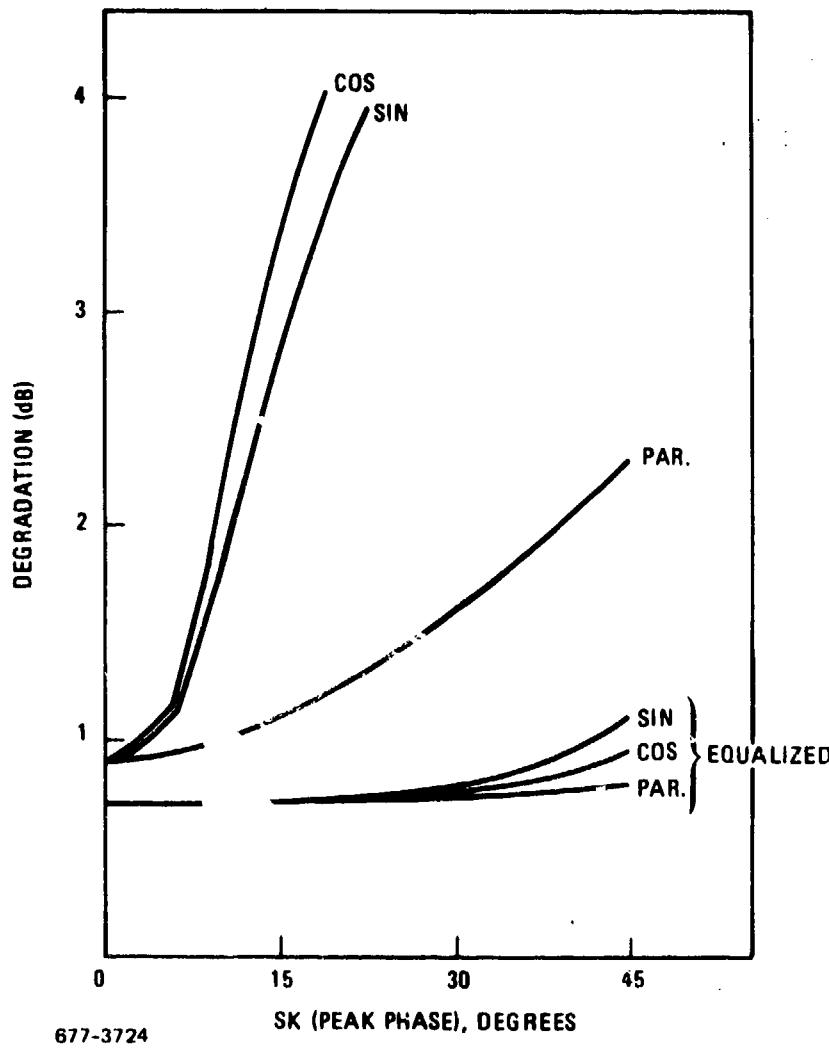
Figure 5-4. Degradation Due to Phase Distortion (BT_b = .333, FR = .333)
E_b/N_o = 10 dB

With FR = 1., and filter bandwidths of BT_b = .333 or BT_b = .4, less
degradation occurs than for the case where FR = .333 since only a fraction of a ripple
occurs over the filter bandwidth for sinusoidal or cosinusoidal phase distortion.
For parabolic phase and FR = 1., the peak phase error over the bandwidth is only
SK/6.25 for BT_b = .4 and SK/9 for BT_b = .333. This is reflected in comparing
Figures 5-3 and 5-4 or Figures 5-5 and 5-6. For FR = 1., and no equalizer, the
degradation due to a given peak phase error (SK) is much less for sinusoidal than for
cosinusoidal phase because the average phase shift over the bandwidth is higher for
cosinusoidal phase than for sinusoidal phase. For FR = .333, the degradations are
more equal since the average phase shifts are similar over the passband. Similarly,
the degradations are less for parabolic if FR = 1.
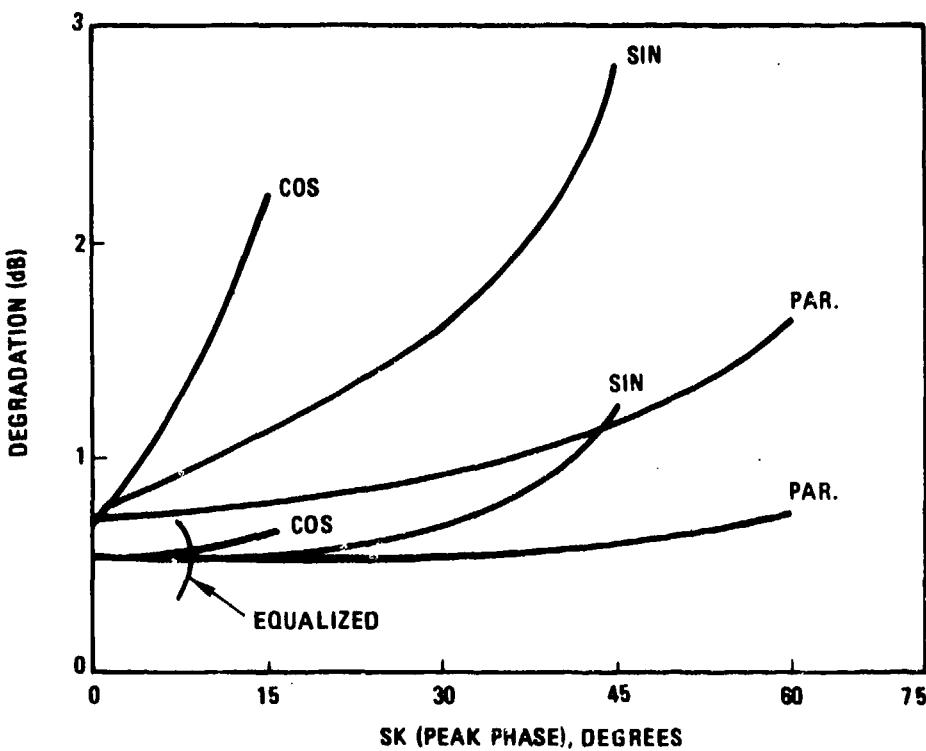
677-3725

Figure 5-5. Degradation Due to Phase Distortion $(BT_b = .4, FR = 1.)$
$E_b/N_o = 10$ dB

In comparing the total degradations for the cases of $BT_b = .333$ and $BT_b = .4$, it is seen that less degradation occurs with the narrow filter for $FR = 1.$, since less phase distortion occurs over the passband. Similarly, equalization is somewhat better with $BT_b = .333$ for $FR = 1.$ For $FR = .333$ and sinusoidal or cosinusoidal phase distortion, somewhat less degradation is incurred for the wider filter than for the narrower. For parabolic phase distortion and $FR = .333$, the wider filter has greater loss since a higher peak phase occurs over the wider pass-band.

With the 8-tap adaptive equalizer and tap spacing equal to T_b^{-1}, degradations were kept very low, close to the degradation due strictly to the equalized filter alone, up to a point at which equalization failed. Failure of the equalizer is due to the use of decision-directed feedback which converges incorrectly when the distortion is sufficient to prevent recovery of the transmitted signal waveform. The level of phase errors at which failure occurs is well above those encountered in the DSCS system. A training sequence could be utilized to insure initial convergence to a point where decision-directed feedback could take over.
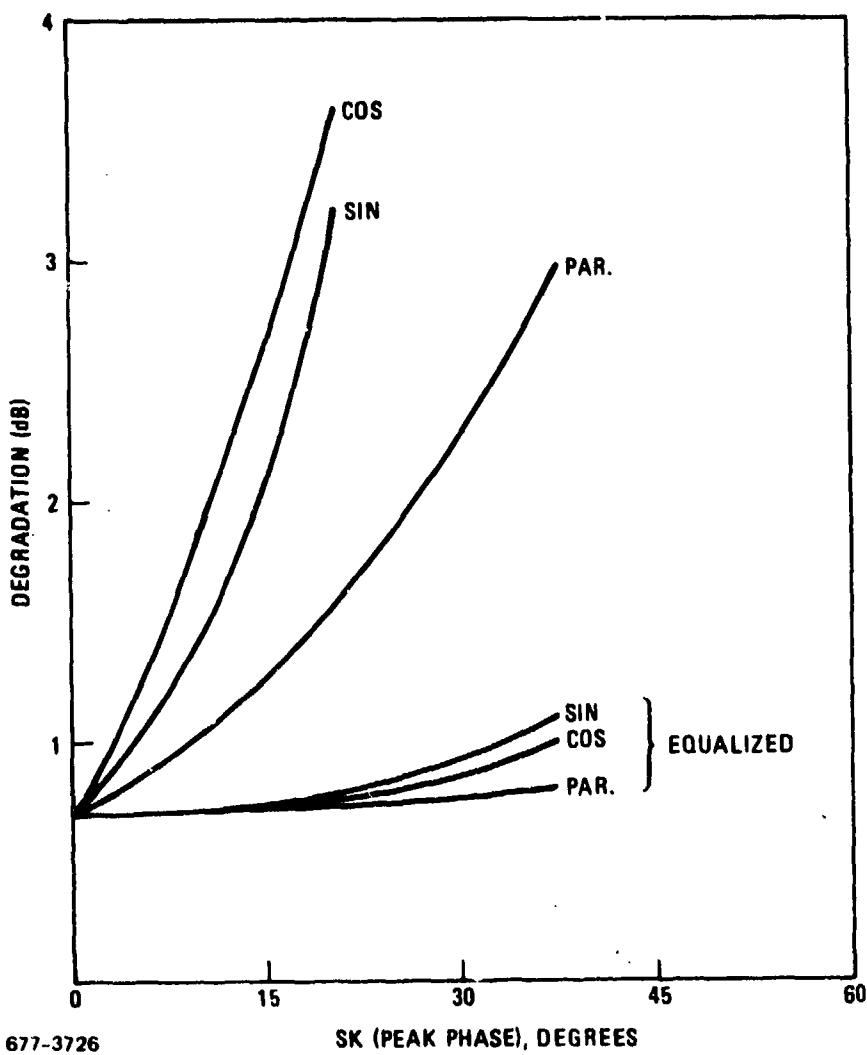
Figure 5-6.   Degradation Due to Phase Distortion (BT_b = . 4,   FR = . 333)
E_b/N_o = 10 dB

Curves are only shown for ripple phase distortions with FR = . 333 and FR = 1. Note that as FR continues to increase, degradation will monotonically decrease. For FR ⋅ . 333, the paired echoes will fall further away, but the degradation will remain essentially the same as that degradation occuring for FR = . 333. Therefore, the values given in the curves for FR . 333 are the worst case conditions for ripple phase distortion for a given peak error SK. The only consideration for lower FR is that with an adaptive equalizer, the number of equalizer taps should be increased to cover the total time spanned by the locations of the paired echoes.

5.1.2.5   Summary of Results

Filters with $BT_b = .333$ permit operation at 3 bps/Hz of bandwidth with low degradation. Filters with $BT_b < .333$ produce rapidly increasing degradation and should not be considered. Minimal degradation occurs around $BT_b = .39$ and degradation increases for wider bandwidths. Adaptive equalization lowers degradation for all BT_b and permits operation over the range $.32 \le BT_b \le .8$ with under 1 dB of degradation in a linear channel.

Duobinary SQPSK is more sensitive to a given level of phase distortion than is conventional SQPSK. Degradation is very large even for 15° peak sinusoidal or cosinusoidal phase distortion, especially for ripple frequencies at or below the filter bandwidth. Higher levels of parabolic phase distortion are tolerated. Adaptive equalization effectively compensates for the effects of phase distortion to the point at which decision-directed equalization fails due to inadequate recovery of the transmitted signal waveform.

Since a given peak level of cosinusoidal phase distortion over the passband produces more degradation than sinusoidal and much more degradation than parabolic phase distortion, it appears beneficial to specify system phase distortion by components rather than simply specifying a total allowable system phase error.

5.2   AM-PM CONVERSION EFFECTS

AM-PM conversion arises in high level power amplification using TWT devices. To separate the effects of TWT amplitude saturation from AM-PM conversion, this section assumes a linear amplitude characteristic and linear AM-PM conversion. The degradation produced by AM-PM conversion on single accessing signals is determined for a range of AM-PM conversion values (from $2^O/dB$ to $8^O/dB$). It is shown that duobinary channels incur more degradation due to AM-PM conversion than results with conventional SQPSK channels. Based on the power level P_i of the complex input waveform $Z_i(t)$, the phase shift φ_p is given by the equation

$$\varphi_p \begin{cases} \varphi_s \cdot 20 \log_{10}(GI \cdot Z_i), & GI \cdot |Z_i|^2 \ge P_f \\ \\ 0 & , GI \cdot |Z_i|^2 < P_f \end{cases} \tag{23}$$

where p_f is a prescribed input backoff power below which no phase shift occurs (at present, $p_f = 0.1$). GI is a gain factor determined by the amplifier drive level desired. Phase ω_s is given in degrees/dB, as shown in Figure 5-7. In operation, subroutine AMP determines the power, p_i, of each input signal sample, z_i, and rotates sample z_i by the required phase shift ω_p.
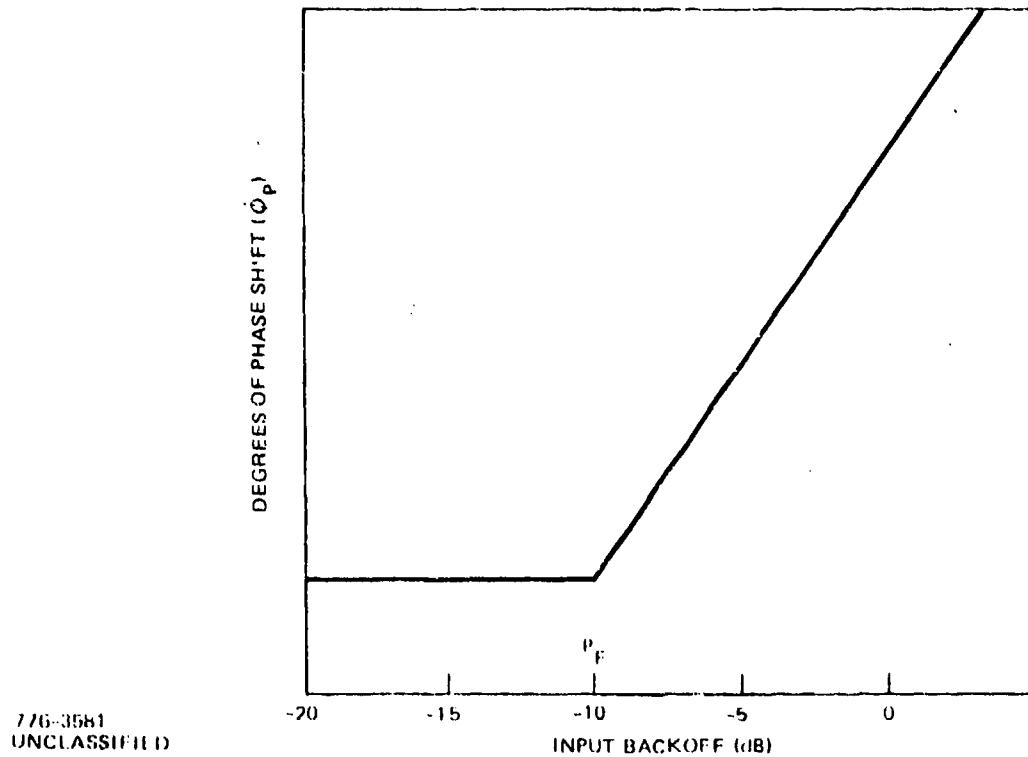
Figure 5-7. Linear AM-PM Conversion Characteristic Assumed

5.2.1 SIMULATION RESULTS

As with the phase distortion simulations, degradations are evaluated at a received $E_b/N_o = 10$ dB for a single transmitted SQPSK signal with AM-PM conversion occurring in the transmitter. Figure 5-1 gives the system modelled. The one-tap phase tracker of Section 3.1 is used in the receiver instead of the adaptive equalizer.

Curves giving the degradation due to AM-PM conversion are in Figures 5-8 and 5-9. Figure 5-8 is based on filters with $BT_b = .333$ while Figure 5-9 assumes filters with $BT_b = .4$. No adaptive equalization was used since its benefits are
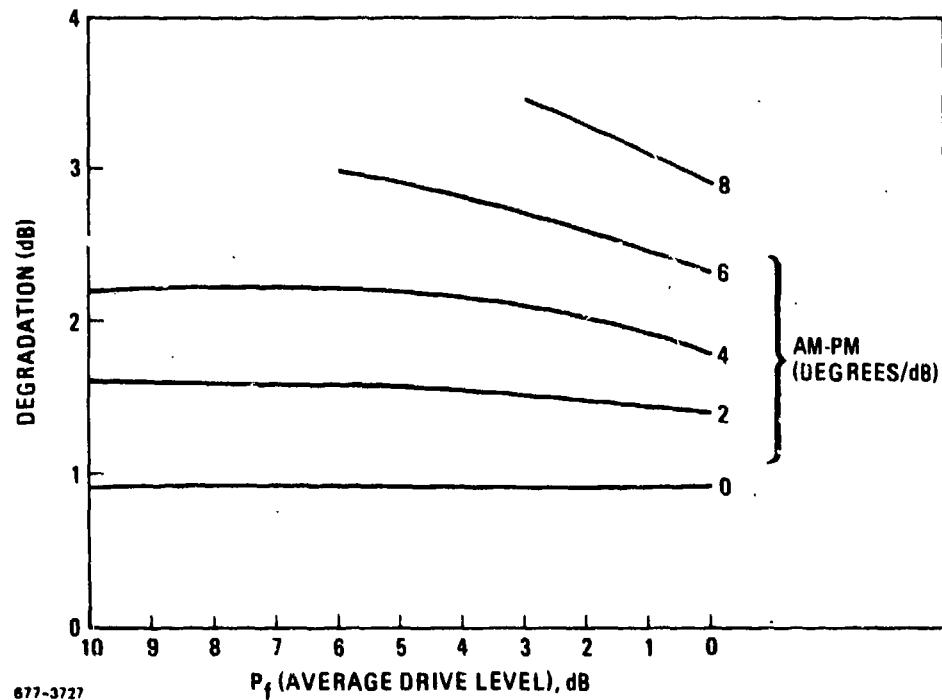
Figure 5-8. Degradation Due to Linear AM-PM Conversion $(BT_b = .333)$
$E_b/N_o = 10$ dB

minimal for AM-PM conversion. The phase shift is specified in degrees per decibel
above a floor below which no phase shift occurs. The abscissa shows the average
drive level, in decibels, above that value at which the linear AM-PM conversion begins.
Linear amplification is assumed for these cases. Comparing these results with the
corresponding degradation to conventional SQPSK channels, as given in the Phase A
Final Report, shows that duobinary SQPSK is more sensitive to a given level of AM-PM
conversion.

5.2.2   SUMMARY

Duobinary SQPSK is more sensitive to AM-PM conversion than conventional
SQPSK, especially for $BT_b = .333$. For $BT_b = .333$, even 4°/dB produces over 2 dB of
system degradation. For $BT_b = .4$, somewhat higher AM-PM levels can be tolerated
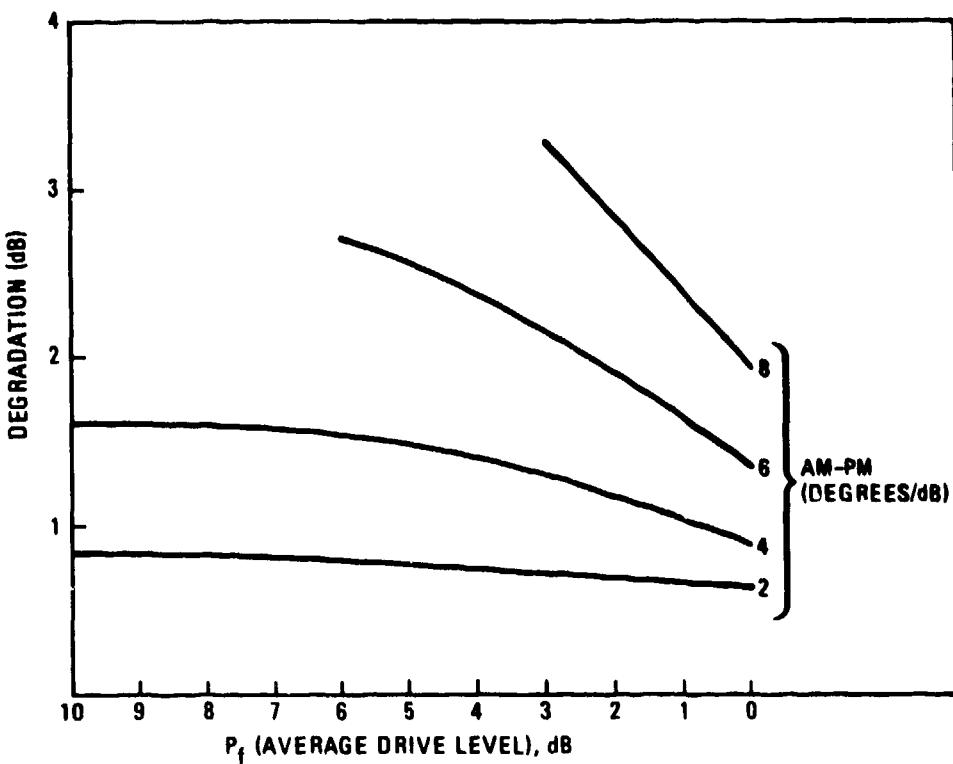
677-3728

Figure 5-9. Degradation Due to Linear AM-PM Conversion (BT_b = .4)
E_b/N_o = 10 dB

for a given level of degradation but AM-PM above 4°/dB imposes heavy penalties on performance. Adaptive equalization is not capable of compensating for the dynamic behavior of AM-PM conversion.

5.3   SINGLE-ACCESS DUOBINARY IN NARROWBAND SATURATING CHANNELS

This section examines the performance and bandwidth requirements for single-access duobinary SQPSK in saturating channels. Efficient bandwidth utilization is a key goal of future TDMA operation in the DSCS. The Phase A study showed that transmission of conventional SQPSK is feasible at rates to 2 bps/Hz of bandwidth while the current study shows that duobinary SQPSK can operate to 3 bps/Hz of bandwidth in a nonsaturating channel. Thus, the duobinary concept appears very attractive for future TDMA operation in the DSCS if a similar efficiency is shown for saturating channels.

Several narrowband saturating channel configurations are modelled. In all cases identical phase distortionless maximally-flat filters are used in the transmitter and receiver. The effects of the Phase III satellite TWT are considered with

regard to the TWT amplitude characteristic, phase characteristic, and composite characteristic shown in Figure A-8 of Appendix A. Degradation is also determined for a soft limiter at the transmitter followed by a narrowband satellite filter and TWT. The effects of the satellite filter bandwidth are evaluated. It is shown that the best tradeoff of degradation and signalling rate occurs when all filters have $BT_b = 0.4$.

The case of an ideal hard-limited transmitter is also evaluated. With a hard-limited transmitter, the satellite TWT can be operated at saturation and the need for power control of the accesses is minimal.

The effects of channel bandwidth on duobinary SQPSK performance were covered in Section 5.1.1. In a linear channel duobinary SQPSK can achieve rates to 3 bps/Hz of bandwidth with under 1 dB of degradation from ideal conventional SQPSK performance and rates to 2.5 bps/Hz with corresponding degradation of only about 0.6 dB. This section shows that these data rates can still be achieved for saturating channels but with an increase in degradation. Degradation decreases as the satellite bandwidth increases.

In addition, the performance of single-access conventional SQPSK is determined for a heavily filtered channel as a function of the Phase III TWT backoff to facilitate a comparison with duobinary performance. Additional curves of TDMA performance with conventional SQPSK are given in the Phase A Final Report.

The overall system modelled is shown in Figure 5-10, although some cases simulated do not include the transmit limiter or the satellite narrowband filter. In all cases considered, the transmit and receive filters are identical phase-distortionless maximally-flat 5-pole filters with (single-sided) BT_b products of 0.333 or 0.4.

All degradations are measured at a received $E_b/N_o = 10$ dB. System degradation is measured by first determining the receiver input E_b/N_o which would produce the same resulting probability of bit error in an ideal ΔPSK system, converting this E_b/N_o to decibels, and subtracting this number from the actual receiver input E_b/N_o used.
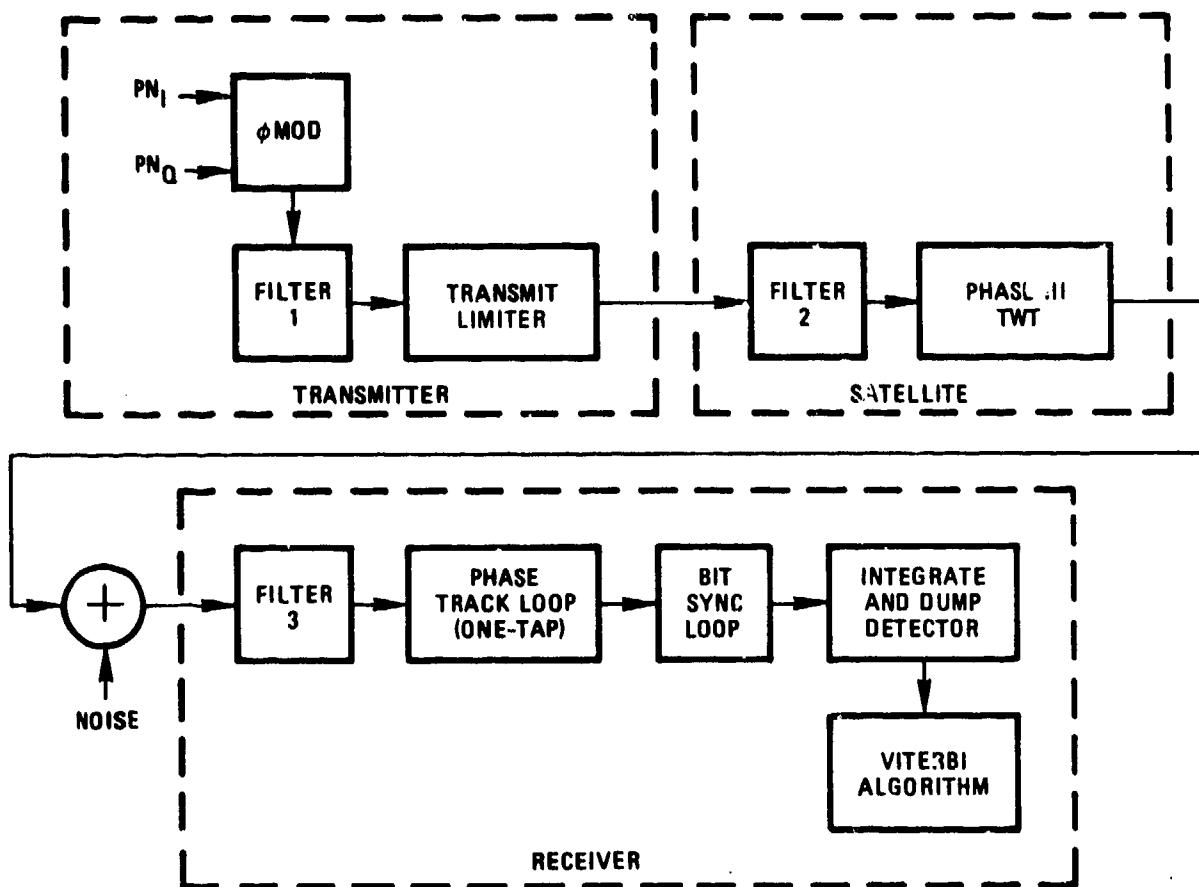
677-3729

Figure 5-10. Overall System Modelled

5.3.1 EFFECTS OF SATELLITE TWT ON HEAVILY-FILTERED CHANNELS

The degradation to duobinary SQPSK in the TDMA mode is determined for the Phase III satellite TWT as a function of output power backoff. The relative contributions to the total TWT degradation of the amplitude saturation and AM-PM conversion are determined separately and the sensitivity of degradation to system bandwidth is evaluated. Identical narrow bandwidth filters are used in the transmitter and receiver. The satellite filter is assumed to be wideband compared to the data rate since no nonlinearity occurs between the transmit filter and the satellite filter. The bandpass preceding the satellite TWT is set by the transmitter filter. Results for maximally-flat filters with $BT_b = 0.333$ are given in Figure 5-11 while the results using filters with $BT_b = 0.4$ are in Figure 5-12. No saturating amplifier is present in the transmitter for these cases.

677-3730
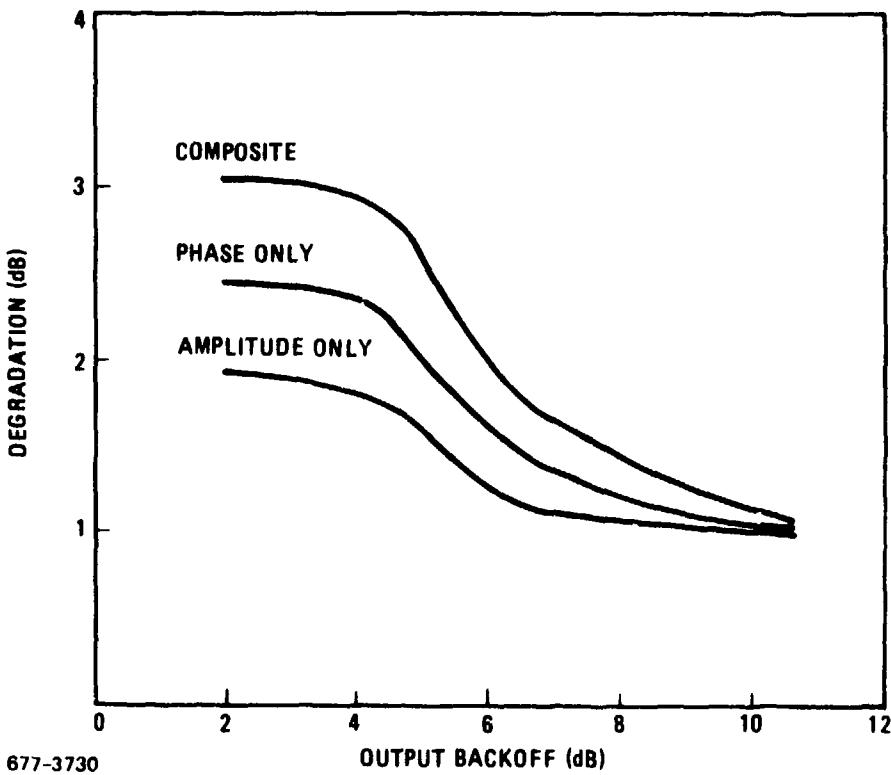
Figure 5-11. Degradation to Duobinary Due to Phase III TWT ($BT_b = 0.333$), $E_b/N_o = 10$ dB

677-3731
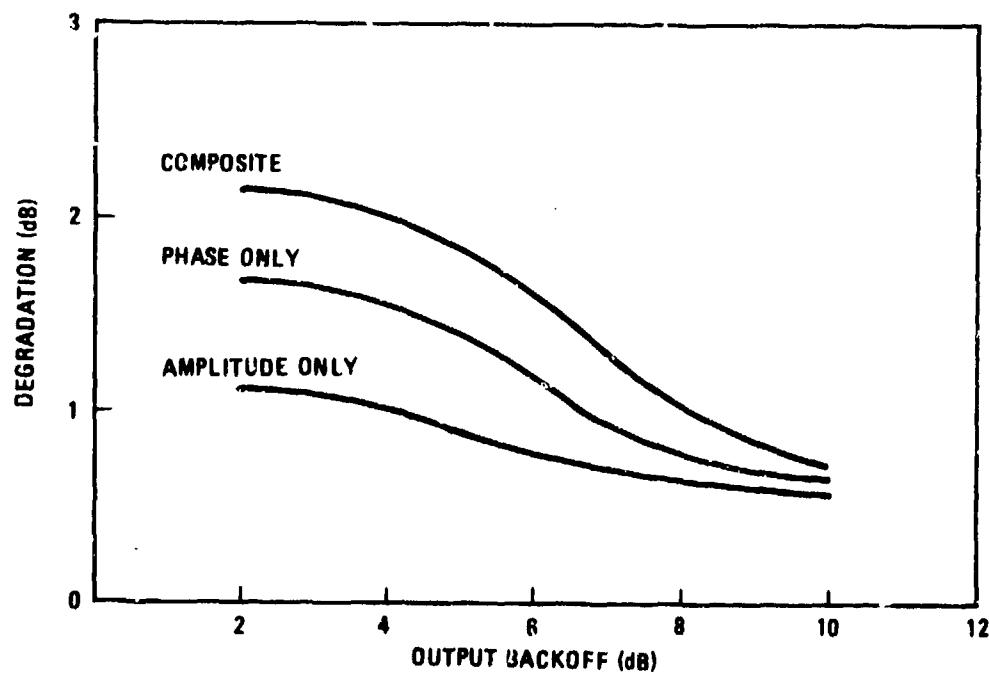
Figure 5-12. Degradation to Duobinary Due to Phase III TWT ($BT_b = 0.4$), $E_b/N_o = 10$ dB

As shown in these results, lower degradation results at all backoff levels of the TWT with filters having $BT_b = 0.4$ than with filters of $BT_b = 0.333$. In addition, the figures show that the major source of degradation in the TWT is due to AM-PM conversion rather than the amplitude nonlinearity.

Figure 5-13 plots the total system loss as a function of the TWT input drive level for a system probability of bit error $= 10^{-5}$. The total system loss is defined as the sum (in decibels) of the output backoff and the performance degradation from ideal ΔPSK performance. The output backoff from saturation represents an effective degradation in the sense that the peak channel power is not available. Note that the total system loss in performance exhibits a nearly constant value over a wide range in TWT input drive level. This insensitivity to drive implies that uplink power control is not very critical to TDMA duobinary performance. Also shown on Figure 5-13 is the TWT output backoff as a function of the input drive level for $BT_b = 0.4$.
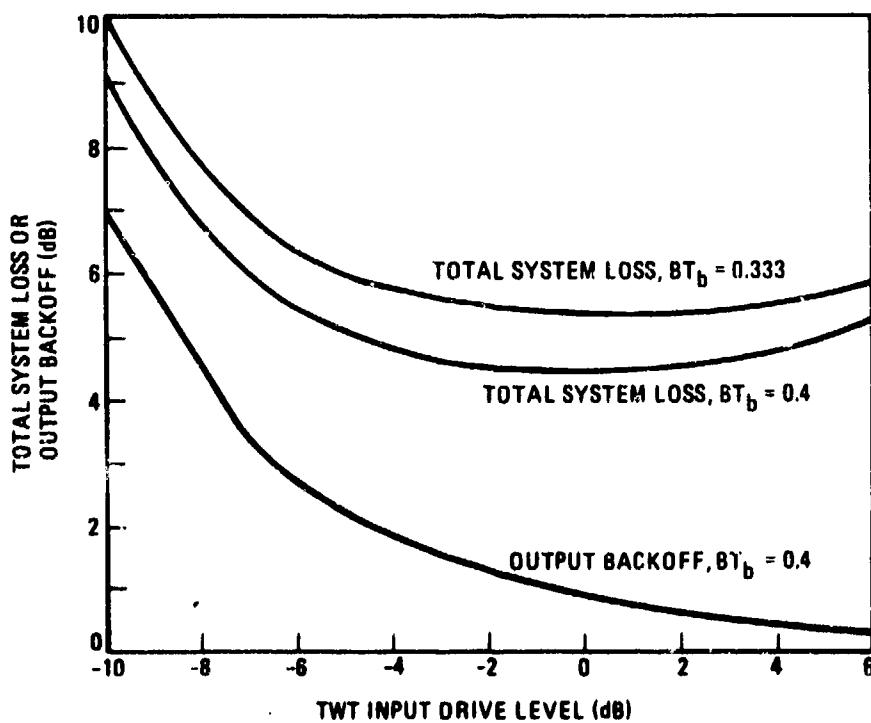
977-5197

Figure 5-13. Total System Loss for Single Access Duobinary Due to Phase III TWT ($P_c = 10^{-5}$)

5-17

5.3.2   INCLUSION OF SOFT-LIMITING TRANSMITTER

This section addresses the topic of duobinary TDMA for DSCS digital communication by postulating saturation in the transmitter as well as in the satellite channel. To take advantage of TDMA by maximizing downlink power and avoiding need for uplink power control of the accesses, it is convenient to have the terminal transmitter drive the satellite channel int' hard limiting. In order to get the requisite uplink EIRP out of smaller terminals to saturate the satellite, 'i.e terminal transmitter may have to operate in a soft- or hard-limiting mode.

A soft limiter is assumed for the transmitter characteristic. The limiter model chosen uses only the amplitude characteristic of the Phase III TWT operated at an ir at backoff of 0 dB, which corresponds to an average output power backoff of approximately 1.2 dB. No AM-PM conversion exists in this transmitter model. The system model is given in Figure 5-10.

Figures 5-14 and 5-15 show the results of having a saturating amplifier in the transmitter, the Phase III TWT in the satellite, and filters in the transmitter, satellite, and receiver. The transmitter and receiver filters are identical zero phase maximally-flat filters of BT_b = 0.333 (Figure 5-14) or BT_b = 0.4 (Figure 5-15) while the bandwidth of the satellite filter is the parameter of interest. Again, these figures show that lower degradation results with transmit and receive filters with BT_b = 0.4 than with BT_b = 0.333. In addition, the satellite filter should be no narrower than BT_b = 0.4 or degradation becomes quite large. Letting all system filters have BT_b = 0.4 gives a good tradeoff between system degradation and bandwidth efficiency. Also shown is a baseline curve with a nonsaturating transmitter to illustrate degradation versus satellite bandwidth in the almost-linear channel.

A measure of system effectiveness is the sum of the output power (decrease in output power from saturation) and the increase in received E_b/N_o to achieve a given error rate at that backoff. This measure is termed the total system loss and the most efficient overall system operation occurs at that output backoff which minimizes this loss.

Figures 5-14 and 5-15 show that the total system loss is minimal when the amplifiers are operated near saturation since the output power increases faster than the increase in E_b/N_o required.

677-3733
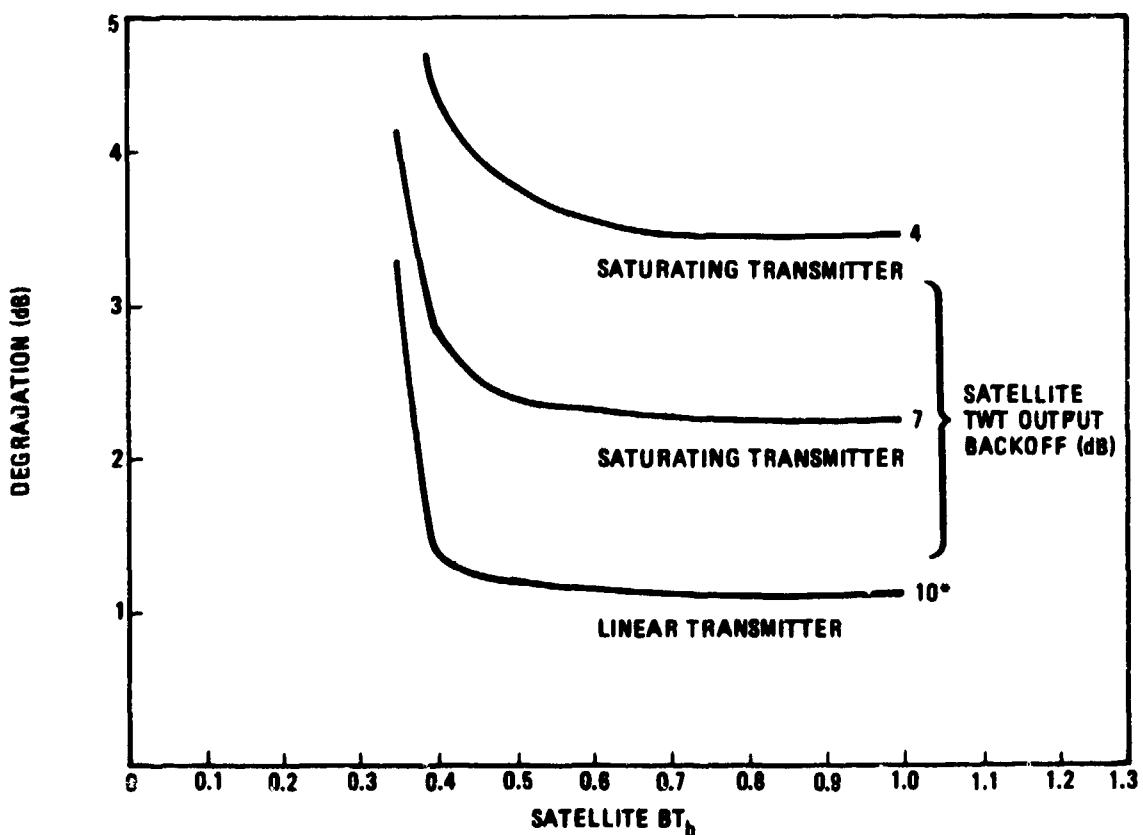
Figure 5-14. Degradation for a Saturating Transmitter and Satellite as a Function of TWT Backoff and Satellite Bandwidth (Transmitter and Receiver $BT_b = 0.333$)

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*Baseline curve with linear transmitter and satellite TWT at 10 dB output backoff.
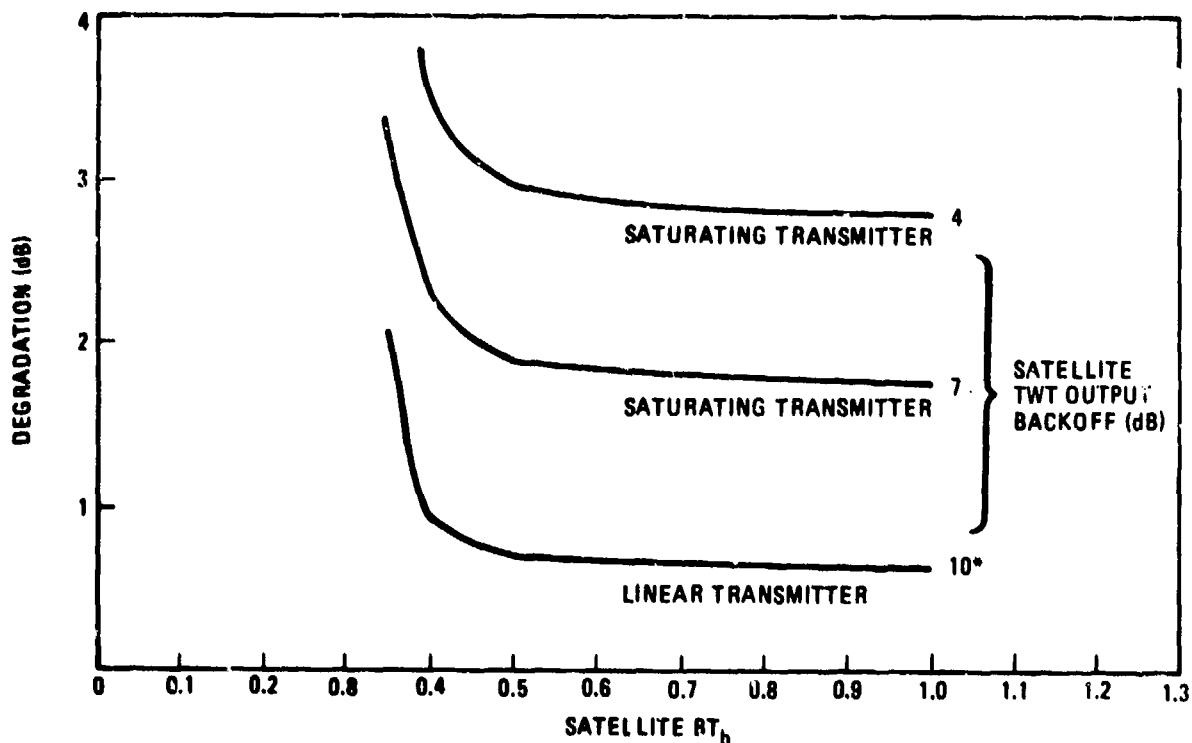
677-3734

Figure 5-15. Degradation for a Saturating Transmitter and Satellite as a Function of TWT Backoff and Satellite Bandwidth (Transmitter and Receiver $BT_b = 0.4$)

5.3.3   INCLUSION OF HARD-LIMITING TRANSMITTER

This section replaces the soft-limiter in the transmitter with an ideal hard-limiter to determine the resulting degradation and the variation in degradation with changes in TWT output backoff. Based on results of sections 5.3.1 and 5.3.2, the transmitter, satellite, and receiver filters are all maximally-flat phase distortionless 5-pole filters with $BT_b = 0.4$. The system modelled is given in Figure 5-10 as before.

Note that duobinary SQPSK has offset bit transitions and corresponding envelope fluctuation, due to filtering, depending on whether a transition actually takes place. The action of the hard limiter boosts the inphase amplitude when a quadrature transition occurs, and vice versa. For SQPSK, the out-of-band spectrum is not restored by hard limiting after sharp cutoff filtering. This is not of particular significance to TDMA unless there is a problem of adjacent channel interference such

*Baseline curve with linear transmitter and satellite TWT at 10 dB output backoff.

as in a channelized satellite repeater.

Figure 5-16 shows the results as a function of TWT output backoff. For a receiver input E_b/N_o = 10 dB, degradation is high but varies only 1.25 dB as the TWT output backoff varies from 2 dB to 10 dB. Degradation is essentially constant for backoffs less than 4 dB. Similarly, a small variation in degradation occurs for the case of receiver input E_b/N_o · 16 dB with changes in the TWT output backoff. This latter case corresponds to a probability of error of around 10^{-5}.

The reason for the small variation in degradation as a function of TWT backoff is apparently due to the action of the hard limiter in maintaining transmitted levels at a constant amplitude. Although the satellite filter partially counteracts this action, the effect is still one of minimizing degradation due to AM-PM conversion in the satellite TWT.
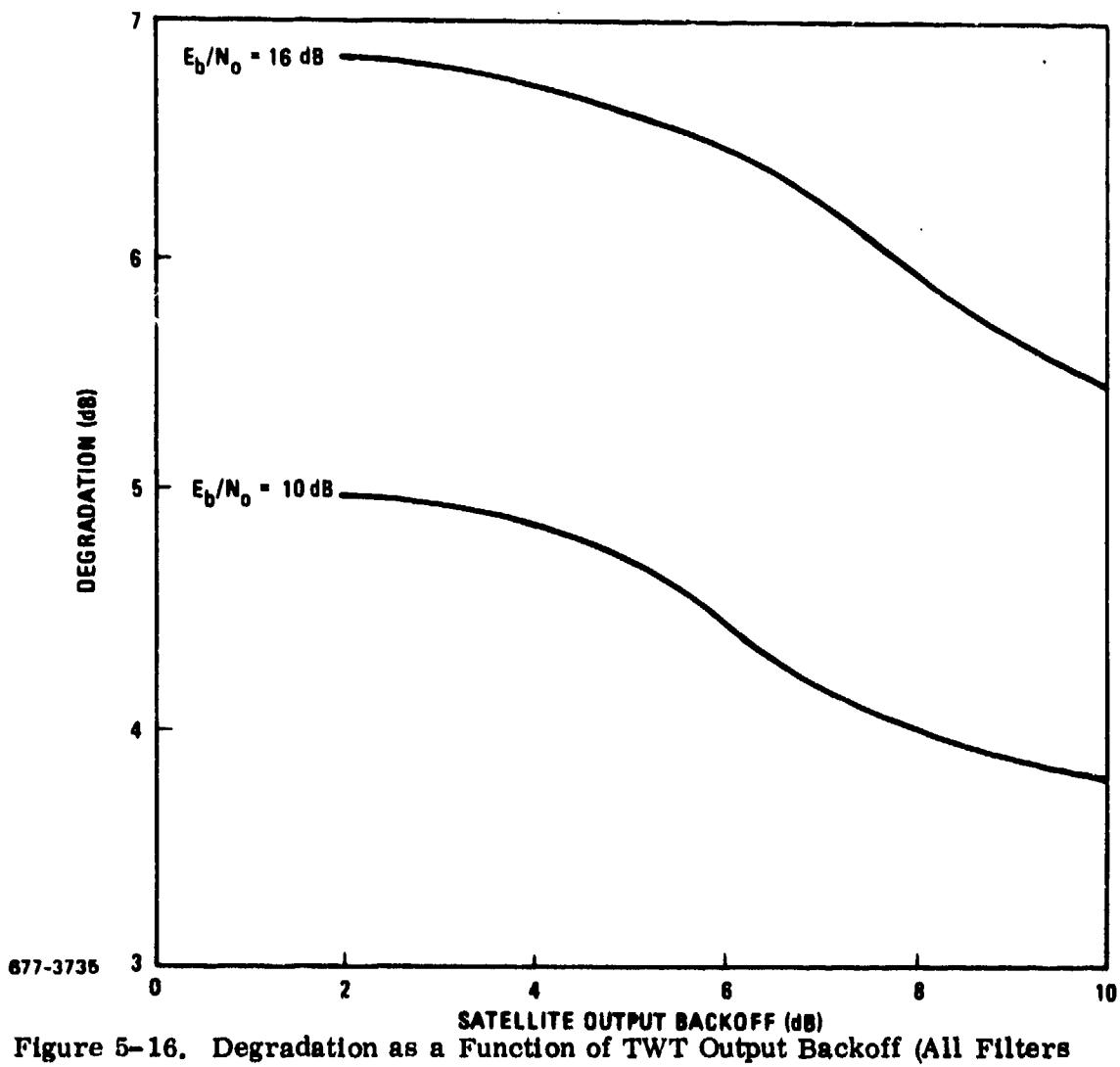
Figure 5-16. Degradation as a Function of TWT Output Backoff (All Filters Having BT_b = 0.4)

The case of TDMA with conventional SQPSK through cascaded non-linearities is treated in Section 8 of the Phase A Final Report. For conventio. .l SQPSK, low degradation in TDMA operation requires that the satellite filter (one-sided) bandwidth be no narrower than $BT_b = 0.6$. For duobinary SQPSK, the corresponding filter can have $BT_b = 0.4$. Thus, TDMA with duobinary SQPSK provides a bandwidth decrease of 50 percent over conventional SQPSK, albeit with an E_b/N_o penalty. If the increased E_b/N_o is feasible, use of duobinary SQPSK provides the better bandwidth utilization for TDMA operation with a hard-limiting channel. Uplink power control is not critical for duobinary TDMA channels containing such limiting amplifiers.

5.4 SINGLE-ACCESS CONVENTIONAL SQPSK IN NARROW BANDWIDTH SATURATING CHANNELS

This section determines the performance of single access conventional SQPSK transmitted through narrow bandwidth channels which include the Phase III satellite TWT to ascertain the degradation that results and the sensitivity of performance to TWT output backoff. Identical filters are placed at each end of the link and signal degradation is determined as a function of the TWT output backoff from saturation.

The channel modelled is shown in Figure 5-17 Only filters with small one-sided bandwidth-time products (BT_b) are used. The selected filters are zero-phase maximally-flat 5-pole filters with $BT_b = 0.5$ or $BT_b = 0.75$ and the equalized filter with $BT_b = 0.5$, plotted in Figure 4-14. For the equalized filter and the maximally-flat filter with $BT_b = 0.75$, an integrate-and-dump detector is used while for the maximally-flat filter with $BT_b = 0.5$, a sampling detector is used. A receiver input $E_b/N_o = 10$ dB is used.

Results are given in Figure 5-18 for single-access SQPSK transmitted through the various filters. As shown, the least degradation occurs for the equalized filter (BT_b 0.5) at all levels of backoff, followed by the zero-phase maximally-flat filter with BT_b 0.75, both assuming integrate-and-dump detection. The highest degradation occurs with the maximally-flat filter (BT_b 0.5) and a sampling detector. *

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*Note that a much higher degradation would have resulted with an integrate-and-dump detector[7].
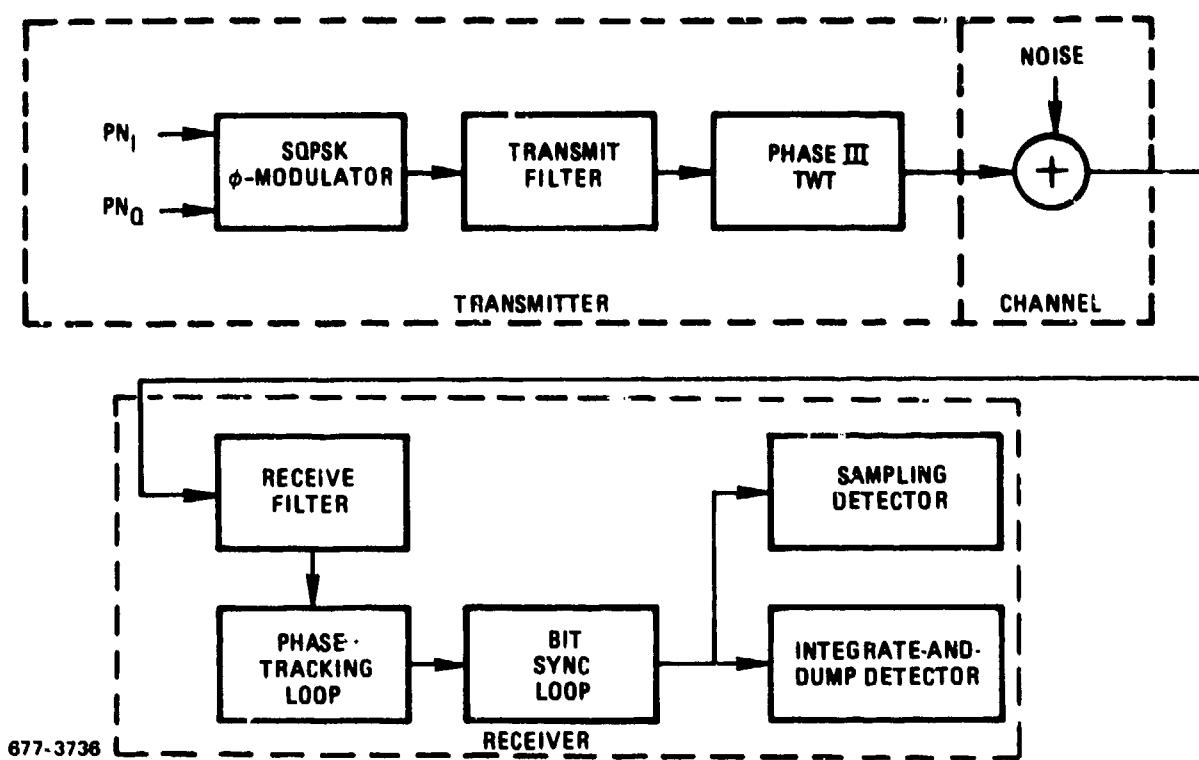
Figure 5-17. Overall Conventional SQPSK System Modelled
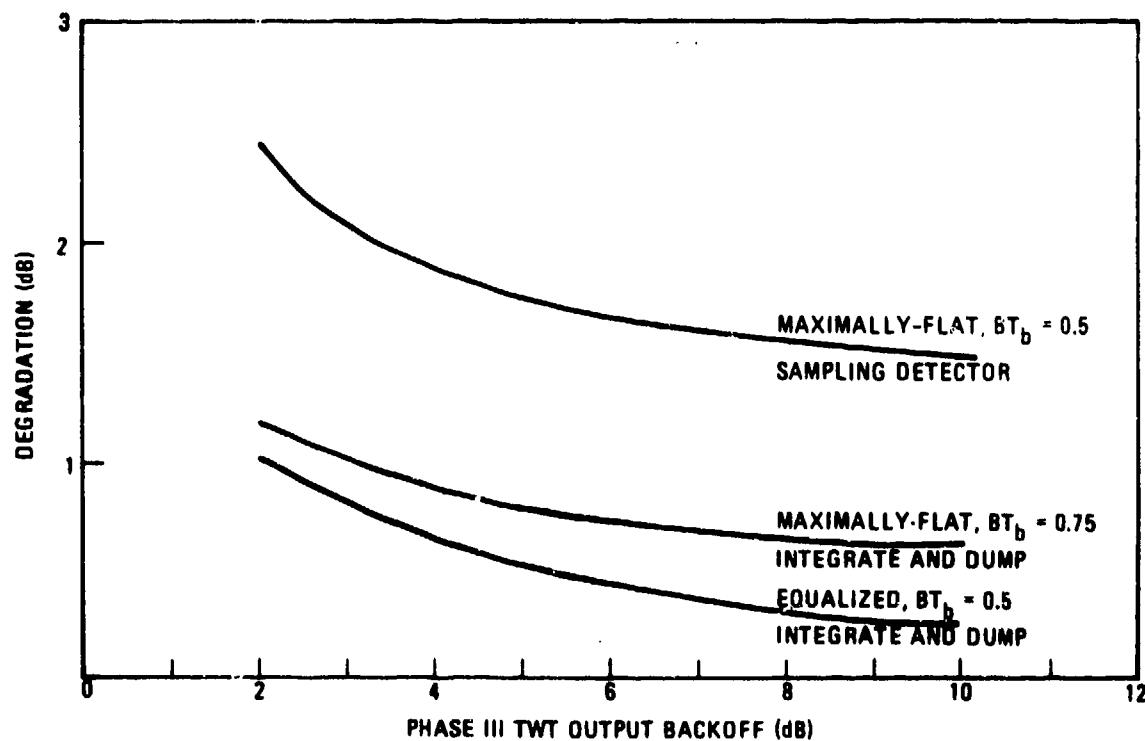
677-3737

Figure 5-18. Single-Access SQPSK Degradation in a Saturating Channel for Various Transmit/Receive Filter Types (E_b/N_o = 10 dB)

Simulations were also performed for conventional QPSK. The results fall just under the corresponding curves for SQPSK. The difference in degradation, even at a backoff of 2 dB, is about 0.2 dB.

If a constant envelope signal were passed through the TWT, no envelope distortion would be produced. With heavy filtering, the envelope can undergo considerable distortion during transitions due to the amplitude saturation and AM-PM conversion produced in the TWT. While degradation rises as backoff is reduced, no major increase in degradation results in these heavily-filtered channels as backoff decreases. This result is in conflict with published measurements[8] which indicated significantly more degradation for heavily-filtered QPSK signals ($BT_b = 0.6$ or less) as backoff decreases.

5.5 TDMA CONCLUSIONS

Use of duobinary signalling for TDMA permits a more efficient bandwidth utilization. With integrate-and-dump detection, phase-distortionless, maximally-flat filters should be used in the transmitter, receiver, and satellite. For the linear channel and wideband satellite, minimum degradation is obtained for filters with $BT_b = 0.4$, with resulting transmission at 2.5 bps/Hz. Filters having $BT_b = 0.333$ permit operation at 3.0 bps/Hz with less than 1.0 dB of degradation over ideal. Use of an adaptive equalizer in the receiver lowers the system degradation, and degradation remains under 1 dB as the transmission rate varies from 1.25 bps/Hz to 3.0 bps/Hz.

Single access duobinary is more sensitive to system phase distortion than is conventional SQPSK. For a given peak phase shift over the filter bandwidth, the highest degradation is produced by cosine distortion, followed by sinusoidal distortion, with the least deterioration in performance produced by parabolic phase distortion. For sinusoidal and cosinusoidal phase distortion with a given peak phase shift, the worst case degradation occurs when one cycle of phase shift occurs over the 3-dB filter bandwidth. Adaptive equalization in the receiver effectively removes the degradation due to phase distortion until that point where the distortion is so severe that the equalizer cannot converge properly under decision-directed feedback error control.

Duobinary SQPSK is also quite sensitive to AM-PM conversion, especially for $BT_b = 0.333$. For this narrow bandwidth, even $4^o/dB$ can produce over 2 dB of system degradation and adaptive equalization cannot remove this degradation.

The major component of degradation produced by a TWT is due to the AM-PM conversion. At zero output backoff and $E_b/N_0 = 10$ dB, the Phase III TWT can produce degradations of 2.1 dB for filters with $BT_b = 0.4$ or 3.0 dB for filters with $BT_b = 0.333$.

For conventional SQPSK transmission through heavily-filtered channels, minimum degradation occurs with the use of equalized filters ($BT_b = 0.5$) in the transmitter and receiver. Inclusion of a satellite TWT in the channel does not produce a major increase in degradation as the backoff is reduced to the saturation level. This insensitivity to output backoff is an advantage of conventional SQPSK over duobinary SQPSK which exhibits a more significant increase in degradation with reduction in backoff for heavily-filtered channels.

If a limiting transmitter and saturating narrowband satellite is assumed for the TDMA system model, degradation increases over the linear transmitter-wideband satellite case. To obtain the highest bandwidth efficiency without a penalty in increased degradation, the use of transmit, satellite, and receive filters with $BT_b = 0.4$ is dictated. This results in transmission at 2.5 bps/Hz.

Although degradation is higher for single-access duobinary SQPSK than for conventional SQPSK, an increase in bandwidth utilization of fifty percent is realized using duobinary for TDMA. The total system loss for duobinary SQPSK accessing the Phase III satellite TWT is relatively insensitive to the uplink power level over a wide range implying that the need for strict power control of the accesses is not necessary.

SECTION VI
PERFORMANCE AND BANDWIDTH UTILIZATION OF DUOBINARY FDMA

Section V showed that use of duobinary SQPSK permits an increase in single-access signalling rate over a heavily-filtered channel, as compared to use of conventional SQPSK transmission. In a similar fashion, this section in estigages the use of duo-binary to maximize bandwidth utilization for FDMA. As an example of the need to increase bandwidth utilization in FDMA operation, consider the situation of the ground mobile forces.

The scenario for the ground mobile forces assumes a large number of duplex FDMA signals. The total channel bandwidth is 45 MHz, and the data rate of each signal is approximately 50 kbps (100 kbps total for duplex signals). One accessing carrier would typically time division multiplex 6 signals; however, this does not affect the computation of bandwidth utilization in terms of number of 50 kbps duplex signals in a specified bandwidth. It is highly desirable to pack as many signals as possible in the channel so that the bandwidth utilization factor is maximized subject to keeping adjacent channel interference to acceptably low levels.

Use of a maximally-flat zero phase shift sharp cutoff 5-pole filter is shown to permit a signal separation of as little as 0.75 times the data rate in a linear channel at data rates of 3 bps/Hz in each channel. A large number of simulation curves are presented for FDMA performance in saturating channels with these filters in the tran mitter and receiver. For both the Phase II and Phase III (Hughes') TWT characteristics, signal separations of between 0.9 and 1.0 times the data rate are feasible with the sharp cutoff filters. The optimal backoff of the TWT amplifiers is found which minimizes the overall system loss in performance. The results are compared with the corresponding results for conventional SQPSK in FDMA operation, as found in Section 7 of the Phase A Final Report.

6.1   SIMULATION CONSIDERATIONS FOR FDMA

This section covers the considerations involved in the selection of channel filters to provide good bandwidth utilization in FDMA duobinary channels using SQPSK signalling. Simulations were performed to determine the system

degradation resulting from adjacent signal interference and intersymbol interference as a function of the signal separation and filtering used. Performance curves are presented as a function of adjacent signal spacing for the narrow bandwidth phase-distortionless maximally-flat filters for (single-sided) BT_b products of 0.333 and 0.4. Identical filters are used in the transmitter and receiver.

In all cases, five duobinary SQPSK signals are used with equal frequency spacing between adjacent signals. Five equally spaced signals generate third-order intermodulation that falls directly on the center channel with a level independent of the level (or presence) of the center signal. This could also be generated using only two equally-spaced signals on one side of the center signal; however, the five signal case more accurately emulates the ground mobile forces scenario. Parameter FCENT determines the signal spacing and is given by the ratio of the absolute value of the frequency separation to the bit rate of the center channel data. Thus, if FCENT = 1, the two inner adjacent channels are located at the first nulls of the center spectra and the two outer channels are symmetrically placed at twice this frequency spacing about the center channel. The bit transition times are staggered by one-eighth of the bit time for each of the five signals and independent PN sequences are used for the signals to minimize cross-correlation effects in the channel.

Spacing FCENT is varied over the range of 4.0 to 0.75 (or wherever degradation becomes severe). Degradation remains constant for FCENT > 1.5 at the value produced by intermodulation and intersymbol interference, since these sources of degradation overwhelm any effects of adjacent signal spectral overlap.

The adjacent channels have either equal power or power 6 dB above that of the center signal for which the probability of bit error is computed. This latter power differential represents a worst case expected value for the ground mobile forces application. For lesser power ratios, the degradation would decrease for close spacings of signals but would remain the same for wide signal separation.

An input signal-to-noise ratio of E_b/N_o 10 dB assumes a noise level low enough that adjacent channel and intersymbol interference tends to dominate. System degradation is measured for the center channel by first determining the receiver input signal-to-noise ratio (E_b/N_o) which would produce the same resulting probability of bit error in an ideal ΔPSK system, converting this E_b/N_o to decibels, and subtracting this number from the actual receiver input E_b/N_o used. Error rates are computed using the estimation procedure of Appendix C.

Automatic gain control (AGC) is used to normalize the total received signal energy to unity at the receiver input. Next, this normalized energy is boosted by the factor β to bring the energy of the center channel to unity to relate the user-specified E_b/N_o to the central signal (for which the probability of bit error is computed). If the composite waveform contains N adjacent signals, with the kth adjacent signal having power P_K and the center channel having power P_C, then

$$\beta = \frac{P_C + \sum_{k=1}^{N} P_K}{P_C} \qquad (24)$$

As an example, for 5 accessing signals with the four adjacent signals each +6 dB above the center signal (for which degradation is determined) N = 4, $P_C = 1$, and $P_K = 4$ (6 dB) for k = 1, 2, 3, 4. Therefore, $\beta = 17$ since the center signal contributes one seventeenth of the total signal power. While this ratio is strictly accurate only when the TWT is operating at large backoff, the suppression effects for low backoff are not large and are therefore not compensated in the normalization process.

Maximally-flat zero phase sharp cutoff filters are used in both the transmitter and receiver, as described in Section 3.5.4 for integrate-and-dump detection. With no channel filtering, the out-of-band energy in the receiver produces high degradation. With only receiver filtering, no attenuation is provided for the adjacent channel spectral energy falling into the receiver passband. The problem becomes even more severe when nonlinearities are introduced into the channel, increasing the magnitude and extent of the interfering spectra. When both transmitter and receiver filtering is employed, the combination suppresses in-band and out-of-band interference sufficiently to produce minor degradation until a spacing at which the filter 3-dB points approach each other. The overall system block diagram is shown in Figure 6-1 and the TWT characteristics used are given in Figures A-8 and A-9 of Appendix A.
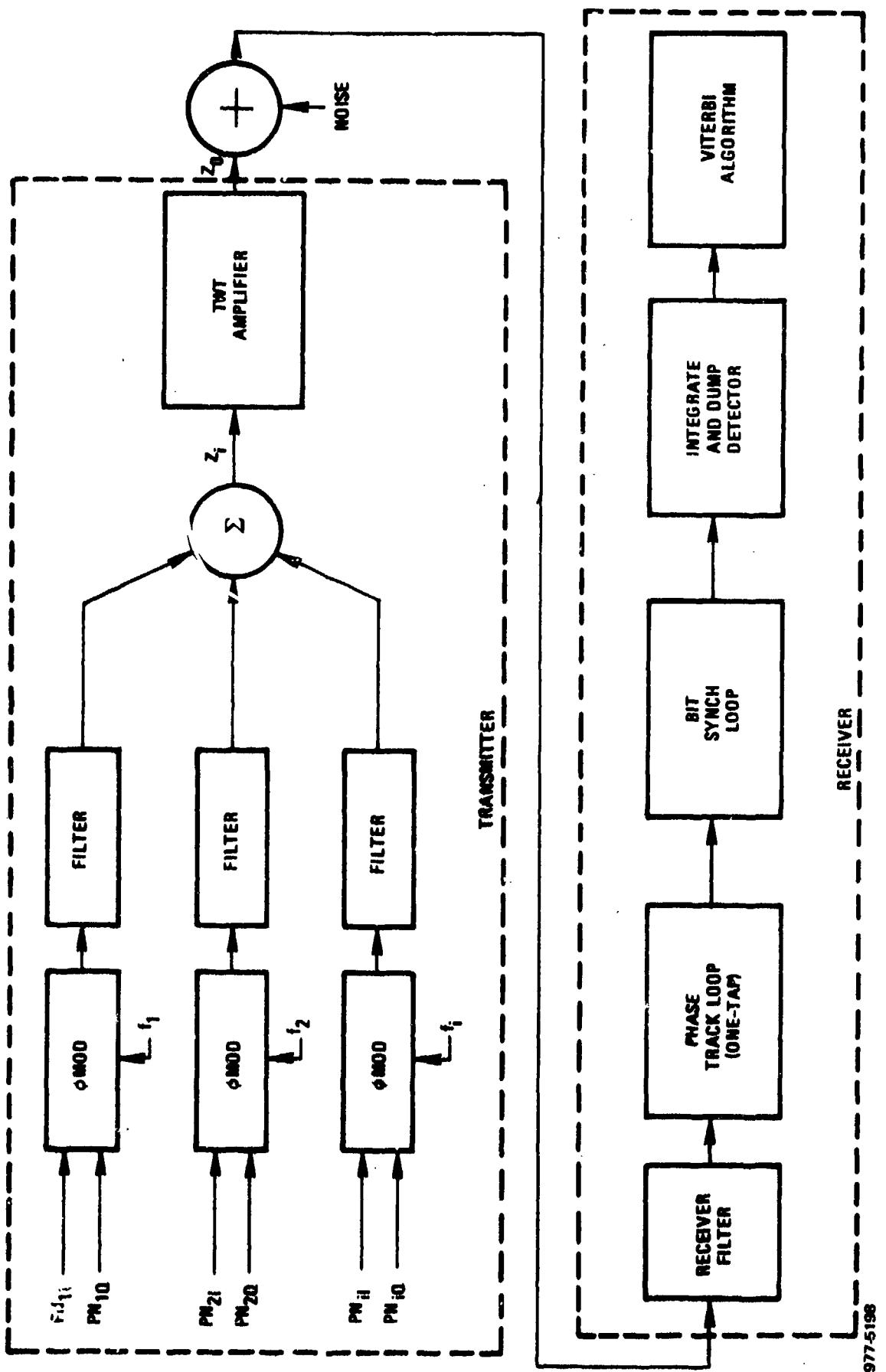
Figure 6-1. Block Diagram of FDMA System Simulated

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6-4

6.2   FDMA PERFORMANCE IN LINEAR (NONSATURATING) CHANNELS

Maximally-flat zero phase shift filters are essentially optimal for use in duobinary channels without equalization, assuming integrate-and-dump detection. With such 5-pole filters in the transmitter and receiver, minimum degradation occurs with $BT_b = 0.4$, corresponding to 2.5 bps/Hz data transmission. Filters with $BT_b = 0.333$ yield slightly higher degradation but permit transmission of single access duobinary signals at 3 bps/Hz. For FDMA operation in linear (nonsaturating) channels, Figures 6-2 and 6-3 give the performance as a function of signal spacing assuming five accessing signals.

Figure 6-2 assumes filters with $BT_b = 0.333$ while Figure 6-3 uses filters with $BT_b = 0.40$. In both figures, two curves are plotted. The lower curve assumes that all accessing signals are of equal power while the upper curve is based on the case of the four adjacent signals each 6 dB stronger than the center signal. The curves merge for FCENT > 1.50. Below this spacing, the greater signal spectral splatter from the stronger adjacent signals introduces more degradation. Comparing Figures 6-2 and 6-3 shows that use of the wider filters produces lower degradation at wide signal spacing where degradation is solely due to intersymbol interference. At close spacings, the narrower filters produce lower levels of degradation since they suppress more of the adjacent channel interference. Use of filters with $BT_b = 0.333$ permits signal spacings of unity with almost no increase in degradation over that due solely to intersymbol interference and spacings down to FCENT = 0.75 are feasible. Performance is better for duobinary than for conventional SQPSK operation in FDMA for channel spacings FCENT < 1.0, but conventional SQPSK produces lower degradation (using equalized filters) for wider signal spacing. Therefore, the decision as to which SQPSK technique to use for a nonsaturating channel depends on the necessity to pack signals as closely together as possible. If maximum bandwidth efficiency is necessary, duobinary is better.

6.3   PERFORMANCE IN SATURATING CHANNELS

This section gives performance for the case of 5 duobinary SQPSK signals simultaneously accessing the DSCS satellite containing either a Phase II or Phase III TWT amplifier. Both the desired case of all signals having equal power and the worst case condition in which the adjacent signals are 6 dB stronger than the center
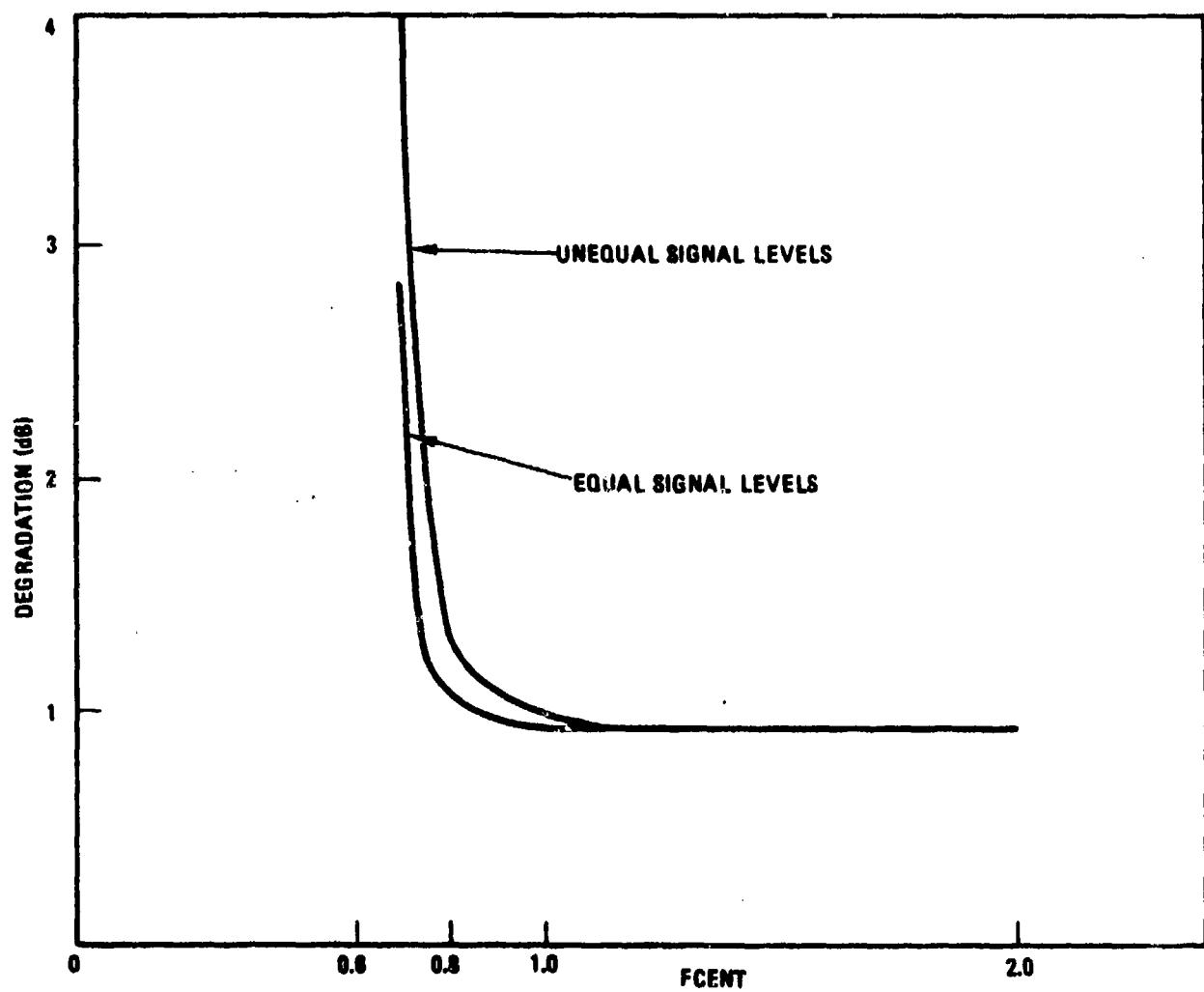
Figure 6-2. Degradation in a Linear Channel ($BT_b = 0.333$)

channel are investigated. Curves are presented as a function of signal separation (FCENT) and TWT output backoff (BO).

Note that the peak power level can be as much as 10 dB above the average output power backoff specified (for the equal power level case). With the TWT models used, the signal peaks are clipped in amplitude for backoffs less than 10 dB. Similarly, the signal peaks receive the maximum phase shift for backoffs less than 10 dB. For the Phase II satellite, this maximum phase shift is 36° while for the Phase III satellite the maximum phase shift is 66°.

Figures 6-4 and 6-5 give the system degradation based on use of the Phase II TWT while Figures 6-6 and 6-7 give the degradation for a Phase III TWT. Figures 6-4 and 6-6 assume 0 dB power differential between the accessing signals.
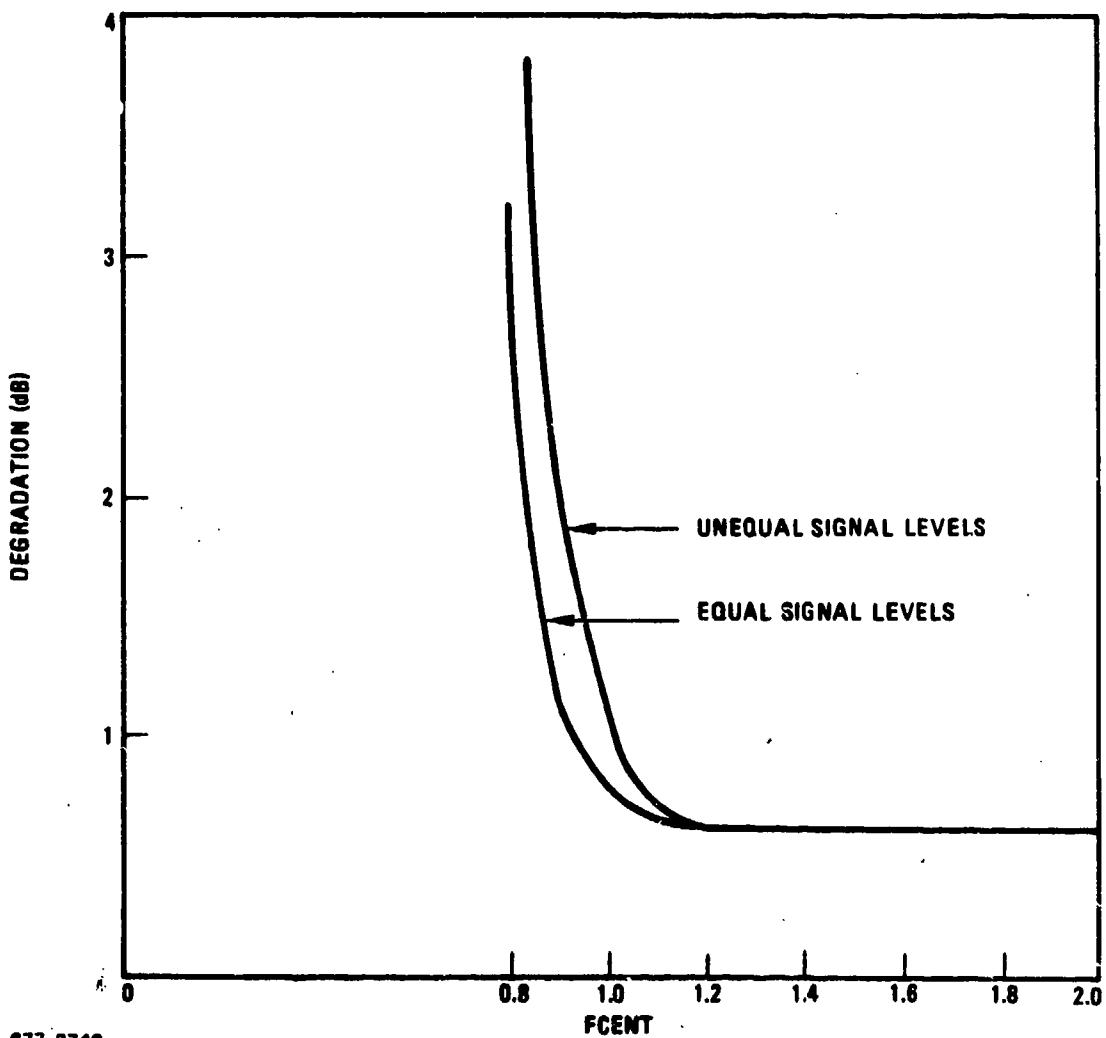
Figure 6-3. Degradation in a Linear Channel ($BT_b = 0.4$)

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Figures 6-5 and 6-7 assume the worst case condition in which the adjacent channels are each 6 dB stronger than the center channel in which degradation is measured. Figures 6-4 through 6-7 use filters with $BT_b = 0.333$.

As shown by the curves, degradation remains constant for FCENT ≥ 1.5 at the value produced solely by intersymbol interference and the intermodulation distortion falling into the center channel. Below FCENT = 1.5, some adjacent channel spectral components begin to fall into the center channel filter passband. The spectrum of each signal has broadened due to the saturation effects of the TWT. This increase in degradation does not become significant compared to the baseline intermodulation distortion degradation until the spacing is reduced below FCENT = 1.
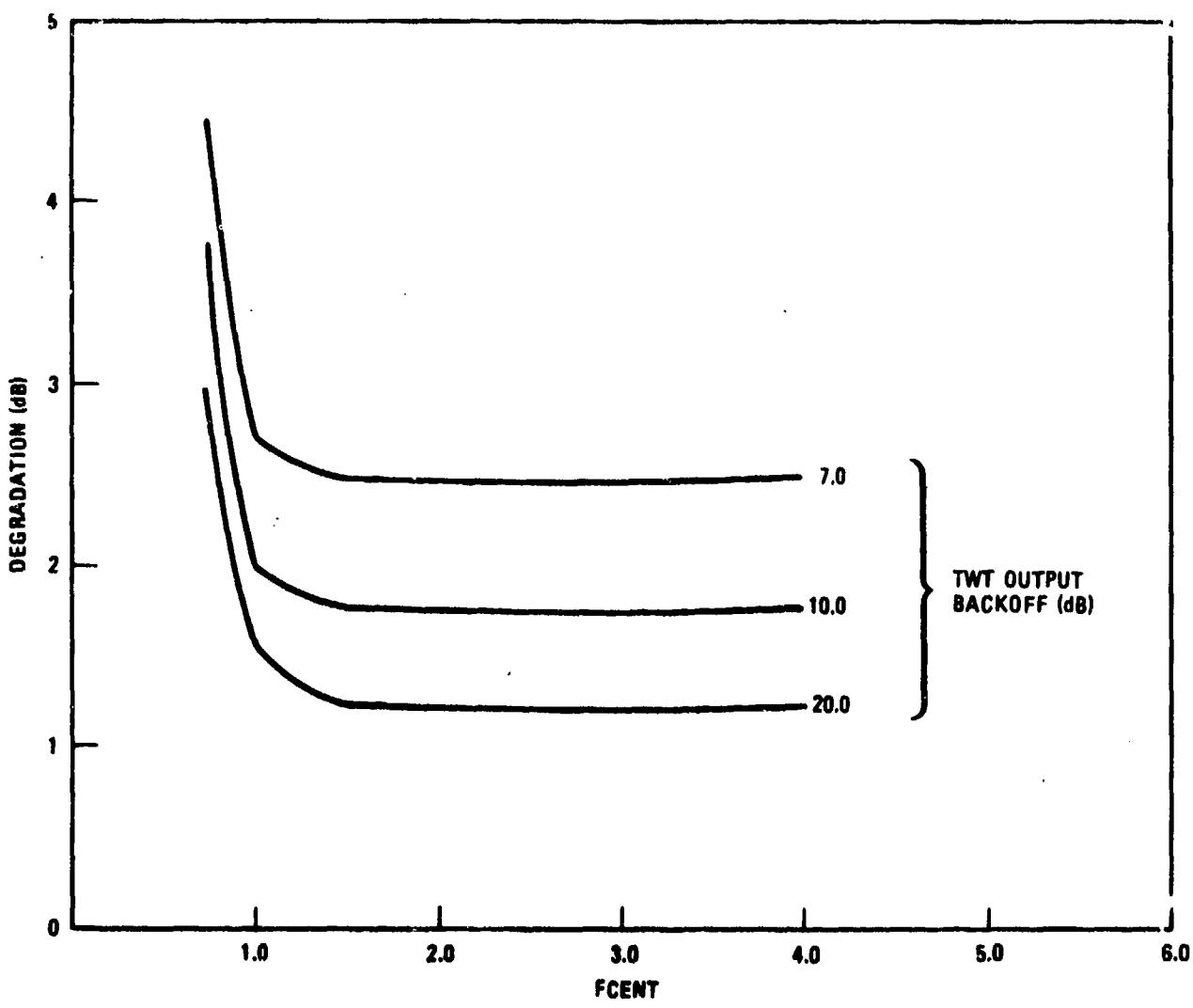
Figure 6-4. Degradation With Equal Signals Through Phase II TWT (BT_b = .333, E_b/N_o = 10 dB)

Figure 6-8 is a repeat of Figure 6-4 with filters of BT_b = 0.4. The major difference is a more rapid increase in degradation for spacings below unity. Similar effects would be observed if Figures 6-5 through 6-7 were plotted assuming the wider filters.

Figures 6-9 and 6-10 illustrate the effect of TWT output backoff on system performance for close signal spacings. All system filters have BT_b = 0.333 and the two figures represent the extremes of system performance.

Figure 6-9 shows the effect of the Phase II TWT output backoff on system performance for a fixed probability of bit error = 10^{-5} and all accessing signals of equal power. In the ideal ΔPSK channel, an E_b/N_o = 9.9 dB achieves this error rate.
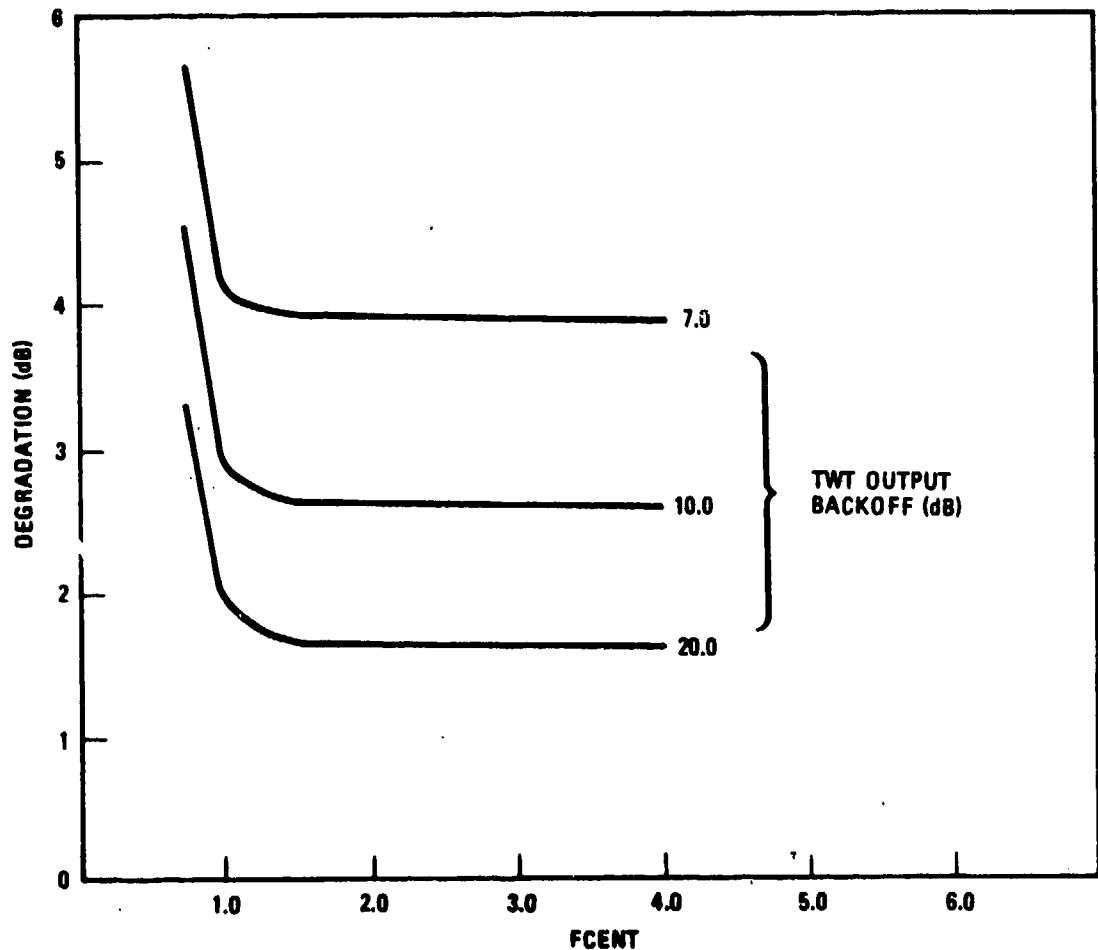
677-3742

Figure 6-5. Degradation With Unequal Signals Through Phase II TWT (BT_b = .333, E_b/N_o = 10 dB)

The total system loss presented here is equal to the sum of the output backoff (decrease in TWT output power from saturation) and the increase in received E_b/N_o (from 9.9 dB) required to obtain the 10^{-5} error rate at that backoff. The minimum value of the total loss represents the most effective backoff for TWT operation. This output backoff is called the turnaround level.

The turnaround level shown in Figure 6-9 occurs around a TWT output backoff of 6 dB although the total system loss remains relatively constant for output backoffs from 5 to 7 dB. The turnaround point is roughly the same for all FCENT in the range 0.8 to 1.0.
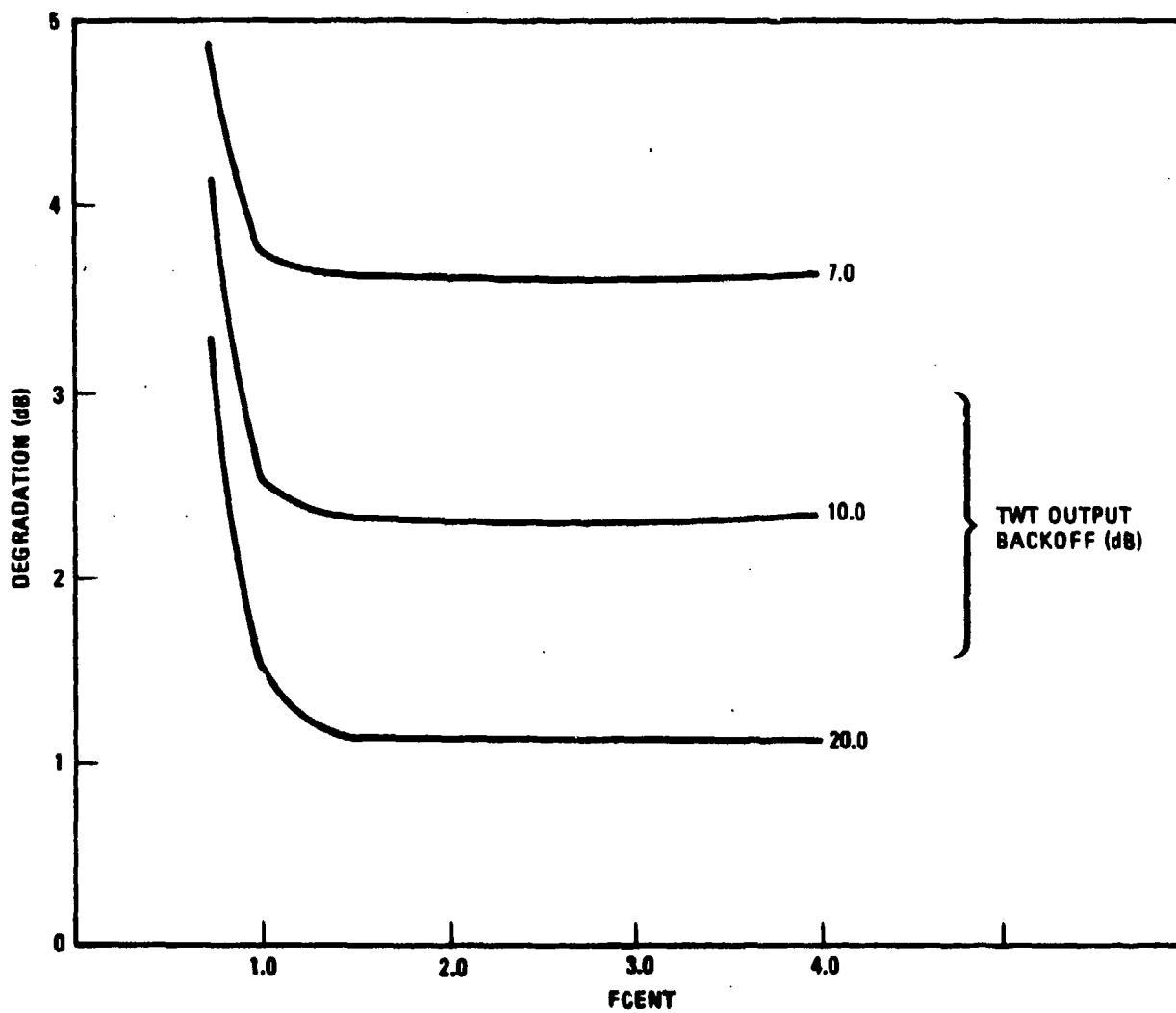
Figure 6-6. Degradation With Equal Signals Through Phase III TWT (BT_b = .333, E_b/N_o = 10 dB)

677-3743

Note that the total system loss shown is valid only for a system error rate of 10^{-5}. For lower error rates, the turnaround would occur at higher backoffs while for higher error rates, the turnaround would occur closer to saturation.

Figure 6-10 shows the total system loss for the case of the adjacent signals each 6 dB stronger than the center channel and operation with the Phase III satellite TWT. This is the worst-case condition. The total system loss is shown for signal separations of FCENT = 0.9 and FCENT = 1.0. For unequal signal levels, turnaround occurs around a TWT output backoff of 6 to 7 dB for an error rate of 10^{-5}. Again, the curves are relatively flat near the turnaround point.
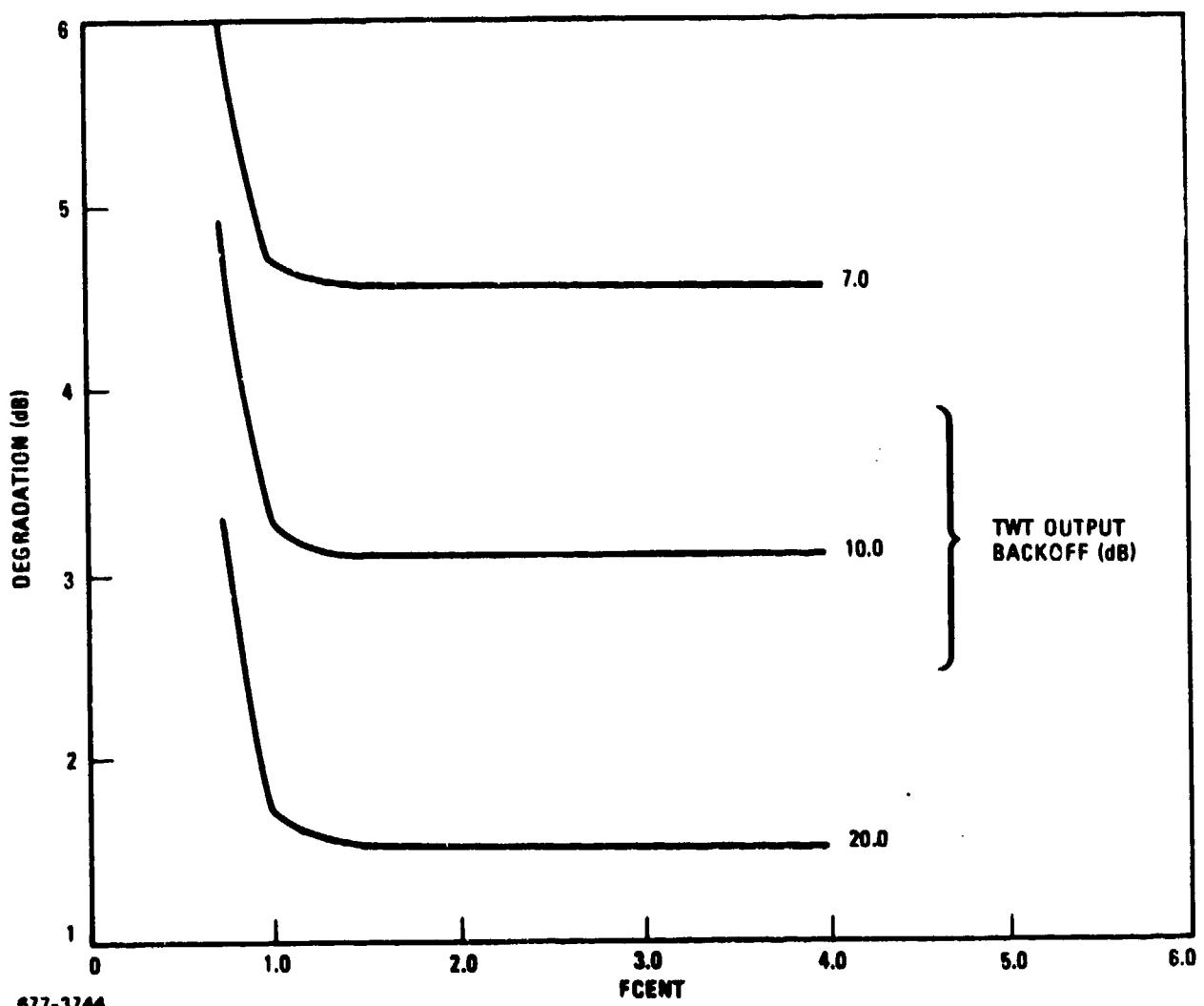
Figure 6-7. Degradation With Unequal Signals Through Phase III TWT (BT_b = .333, E_b/N_o = 10 dB)

677-3744

Comparing these results with the comparable results for conventional SQPSK in FDMA operation (Section 7 of the Phase A Final Report) shows that the use of duobinary SQPSK permits a signal separation to FCENT = 0.9, which is below the required separation of 1.1 for conventional SQPSK using equalized filters with BT_b = 0.5. Duobinary SQPSK, however, requires that the TWT be operated at about a 3 dB greater output backoff than conventional SQPSK in order to minimize the total system loss.
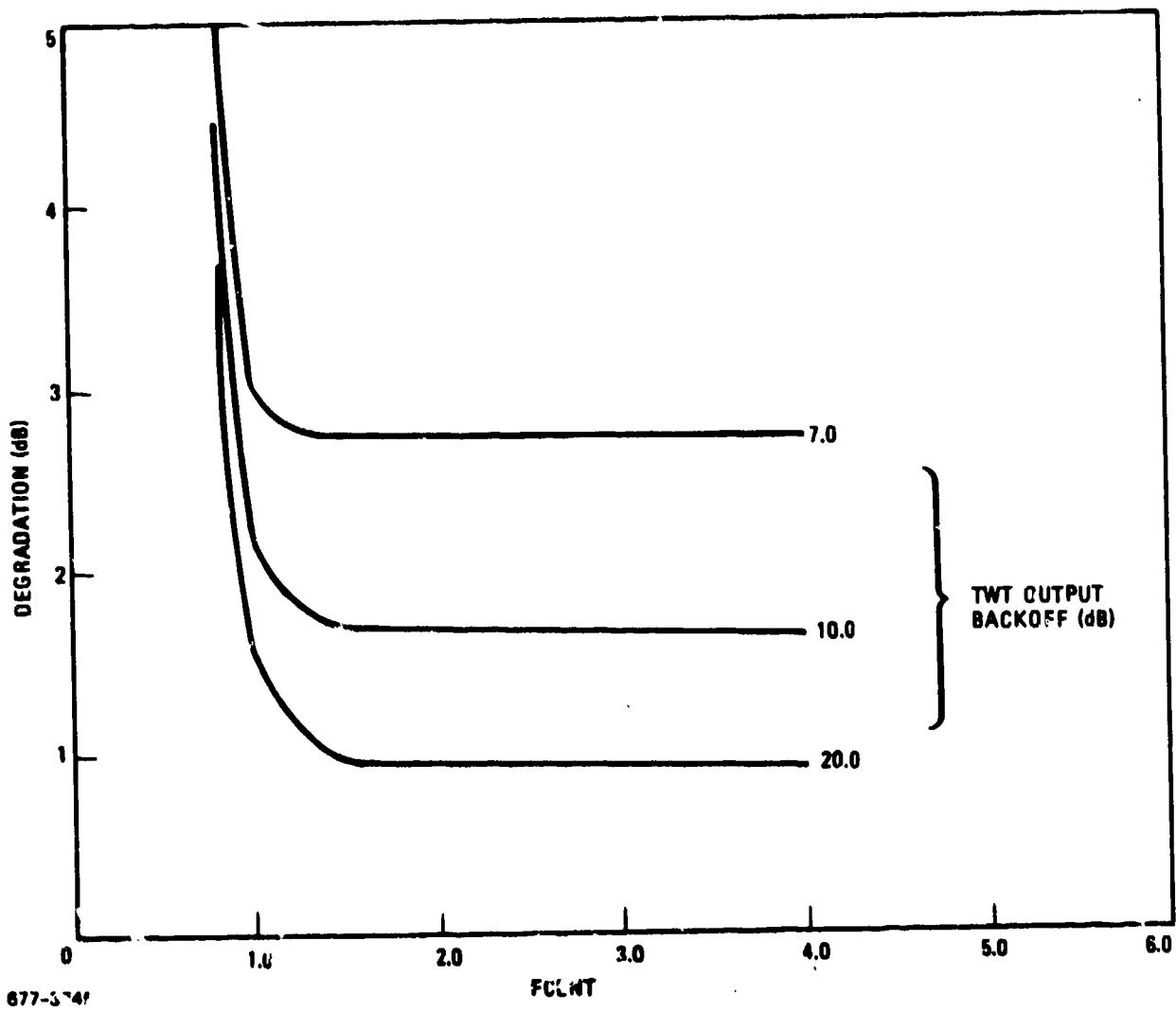
677-3741

Figure 6-8. Degradation With Equal Signals Through Phase II TWT ($BT_b = 0.4$, $E_b/N_o = 10$ dB)
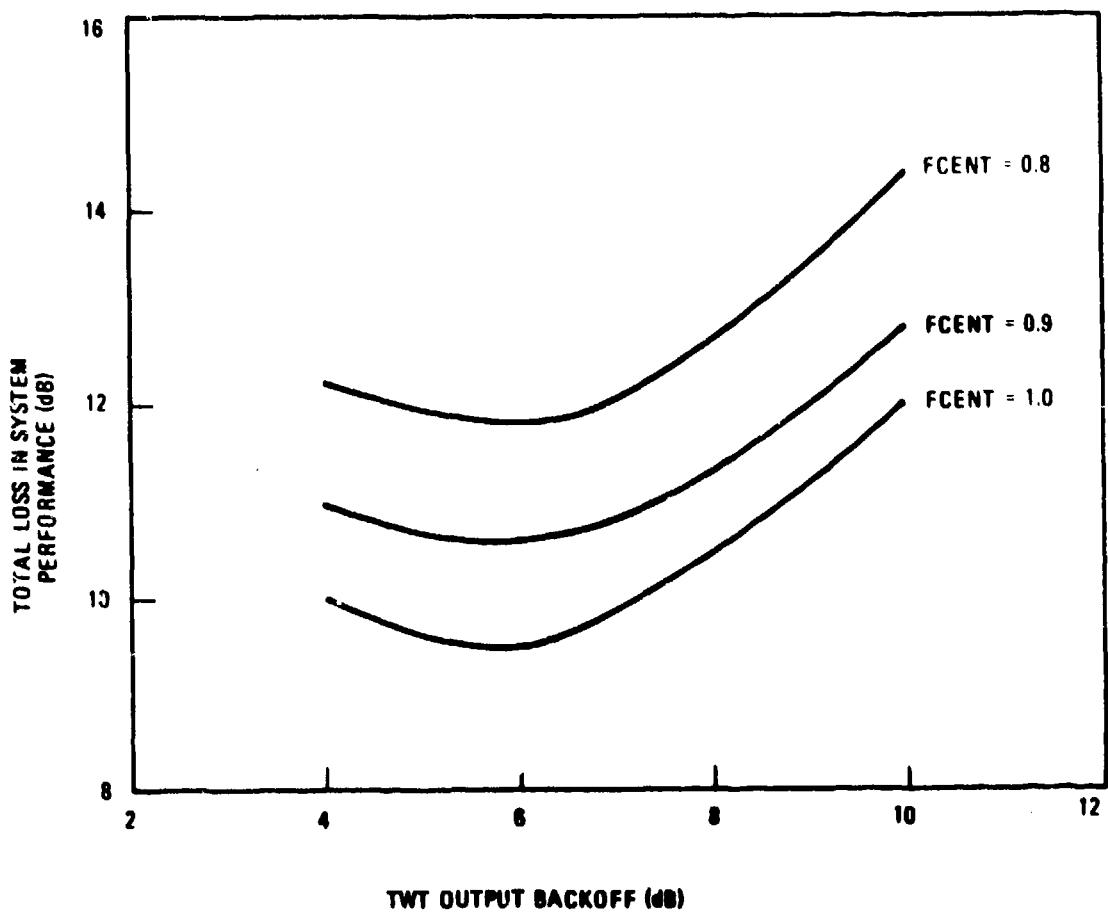
Figure 6-9. Total System Loss at $P_e = 10^{-5}$ (Phase II TWT, Equal Signal Levels, $BT_b = .333$)

677-3746

TWT OUTPUT BACKOFF (dB)
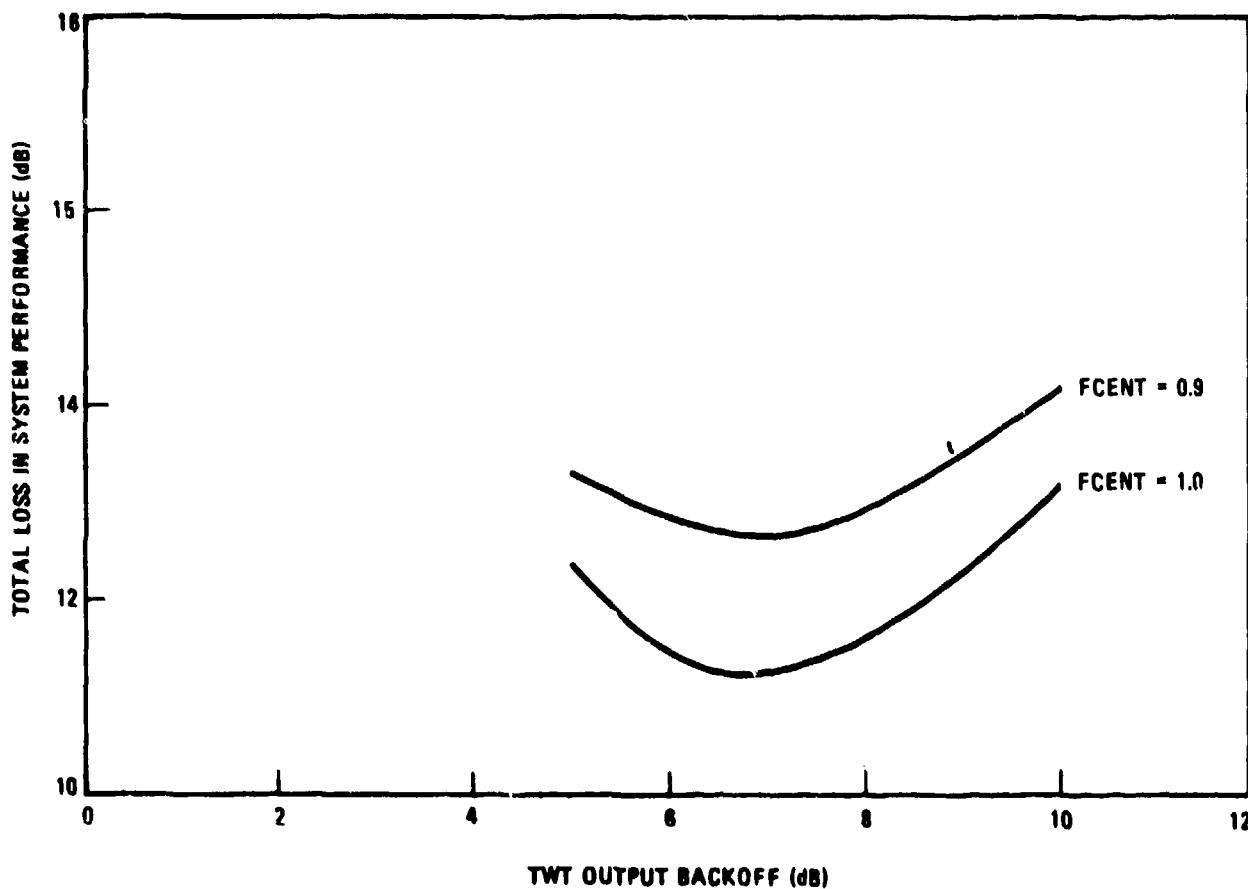
677-3747

Figure 6-10. Total System Loss at $P_e = 10^{-6}$ (Phase III TWT, Unequal Signal Levels, $BT_b = .333$)

6.4   DUOBINARY PERFORMANCE WITH ADJACENT CHANNELS CONTAINING CONVENTIONAL SQPSK

This section evaluates the performance and bandwidth efficiency of an FDMA scenario in which the center channel is duobinary SQPSK and the adjacent channels are conventional SQPSK. Performance is monitored in the center (duobinary) channel. This scenario emulates a mix of transmission schemes assuming that some users switch to duobinary signalling while others continue to use current SQPSK equipment.

Results are obtained for both a linear channel and for a saturating (Phase III TWT) channel as a function of signal separation FCENT. * The optimal FDMA transmitter filters are used for the appropriate signalling; i.e., equalized filters, Figure 4-14, with $BT_b = 0.5$ for the conventional SQPSK and zero-phase maximally-flat filters with $BT_b = 0.333$ for the duobinary SQPSK. The receiver filter is a zero phase maximally-flat filter with $BT_b = 0.333$. The system modelled is given in Figure 6-1. A receiver input $E_b/N_o = 10$ dB is used in the simulations.

Figure 6-11 gives results for the linear channel for the case of five equal-level signals and the worst-case condition in which the adjacent conventional SQPSK signals are each 6 dB stronger than the center duobinary channel. For the equal signal case, spacings down to FCENT = 0.9 produce acceptably low degredation while degradation rises rapidly below this point. Note that the 3 dB bandwidth of the adjacent channels meet the 3 dB bandwidth of the duobinary center signal at a spacing of FCENT = 0.833. For this worst-case condition, spacings to 0.95 (or less) are acceptable. If higher degradation can be tolerated, spacings somewhat below this can be obtained. Note that in the linear FDMA channel with only duobinary signals and filters with $BT_b = 0.333$, spacings down to 0.75 (or less) are realizable. Conversely, for FDMA with all signals conventional SQPSK, spacing should be no closer than 1.10.

Figure 6-11 also gives the comparable performance when these five (equal-level) accessing signals pass through the Phase III satellite TWT. Degradation remains at the level given by combined intersymbol and intermodulation distortion until a spacing of FCENT = 1.2. As spacing is reduced below this level, degradation rises due to adjacent channel spectral overlap, but operation is possible to FCENT = 1.1. The adjacent channel spectra have been broadened due to the nonlinear effects of the TWT.

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*The duobinary and the conventional SQPSK signals have equal data rates in the current simulation.

6-15
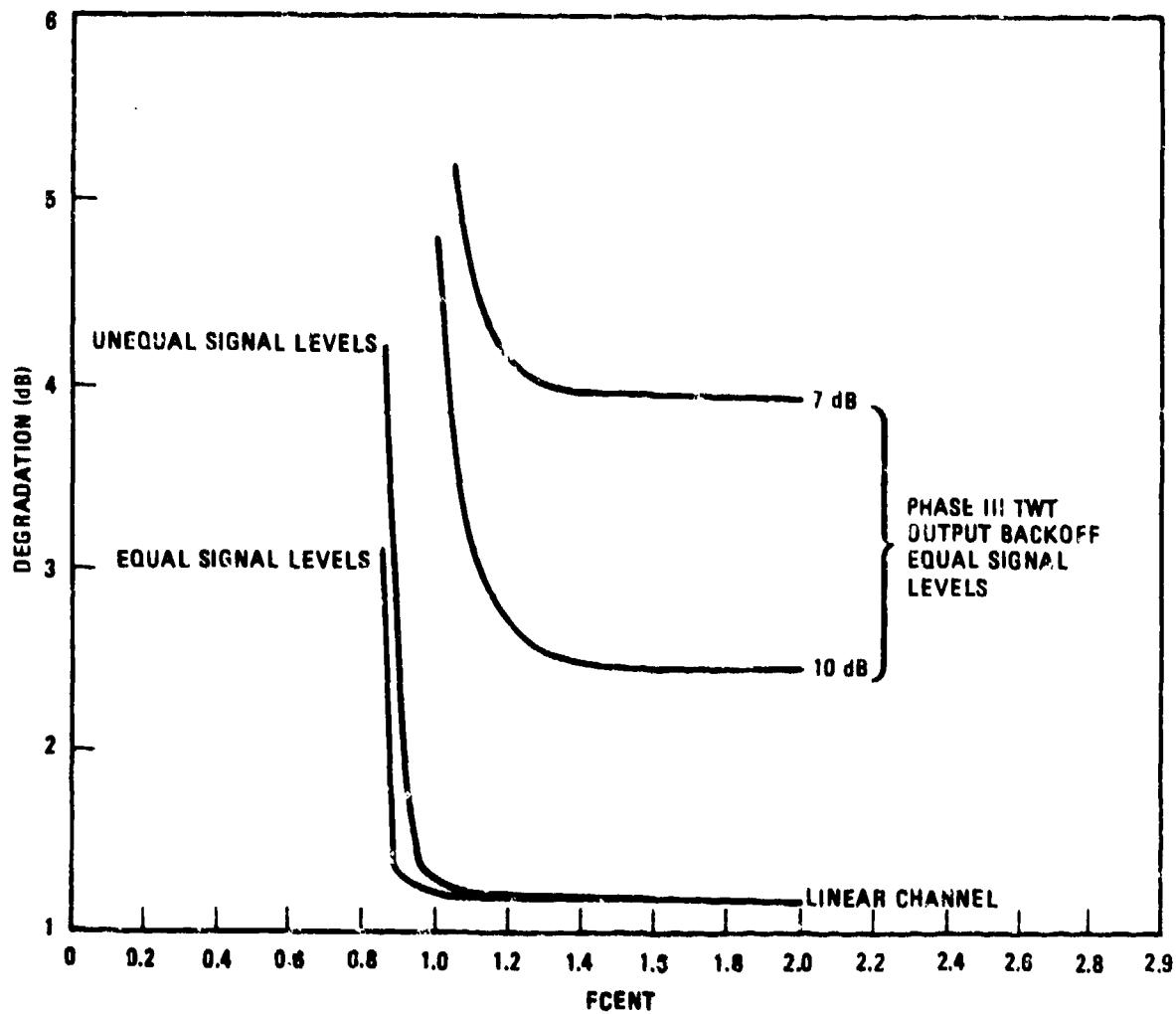
Figure 6-11. FDMA Degradation in Duobinary Channel With Adjacent Signals Conventional SQPSK (E_b/N_o = 10 dB)

These results can be compared with Figure 6-6 which is the comparable case with five duobinary signals accessing the Phase III TWT, all filters being zero-phase, maximally-flat with BT_b = 0.333. For this case, the baseline degradation due to intersymbol and intermodulation distortion is about 0.2 dB less than shown in Figure 6-11 for the mixed signal case. For all duobinary signals, degradation begins to rise rapidly at the spacing FCENT = 1.0. The corresponding case of five conventional SQPSK signals accessing the Phase III TWT, with equalized filters having BT_b = 0.5, is given in Figure 7-32 of the Phase A Final Report. The baseline degradation is below that of Figure 6-11 and dips to a minimum at FCENT = 1.3. Degradation increases rapidly below this spacing.

6.5   CONCLUSIONS

Duobinary SQPSK is feasible for use in FDMA operation, both in linear and saturating channels although coding is not desirable for duobinary, as shown in Section 4.4. Therefore, only uncoded duobinary SQPSK is considered here for FDMA operation. Closest signal spacing is realized with transmit and receive filters having $BT_b = 0.333$. This permits the packing of signals, each having a data rate of 3 bps/Hz, at spacings to FCENT = 0.75 (or less) in linear channels or 0.90 if TWT amplifiers are included. This compares to the use of conventional SQPSK with transmit and receive equalized filters having $BT_b = 0.5$ where each signal has a data rate of 2 bps/Hz with spacings to 1.10* in a linear or saturating channel. Thus, use of duobinary SQPSK implies an improvement in bandwidth utilization of between 25 and 50 percent compared to conventional SQPSK for FDMA. On the negative side, the Phase II or Phase III TWT has to be operated at about a 3 dB greater backoff with duobinary SQPSK to achieve the same degradation levels as realized by conventional SQPSK. Turnaround occurs in the range of TWT output backoff between 5 and 7 dB for duobinary SQPSK operation.

Duobinary can be mixed with conventional SQPSK signalling in FDMA systems. Assuming all signals have the same data rates and the optimal filters are used for both types of signalling ($BT_b = 0.333$ for duobinary and $BT_b = 0.5$ for conventional SQPSK), spacings down to at least 0.9 are adequate between the duobinary and conventional signals in the linear channel. This corresponds to minimum spacings of 0.75 for all-duobinary TDMA and 1.10 for all-conventional SQPSK-TDMA operation. For the case of these (equal level) signals accessing the Phase III satellite, a spacing of 1.2 is adequate between the duobinary and adjacent conventional SQPSK signals. For all-duobinary TDMA accesses, spacings to 1.0 are possible while spacings to 1.3 are feasible for the case of all-conventional SQPSK accesses through the Phase III satellite TWT.

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*Minimum degradation occurs at a spacing of 1.30.

SECTION VII
CONCLUSIONS AND RECOMMENDATIONS

7.1   CONCLUSIONS

This section summarizes the major conclusions reached during this study, based on extensive analyses and computer simulations.

- If the channel is linear (i.e., non-saturating) and is adaptively equalized to approximate the ideal duobinary response, a data rate of 3 bps/Hz can be achieved by SQPSK transmission. The receiver utilizes the Viterbi algorithm for optimal duobinary demodulation of the heavily filtered signal. In this report, this mode of operation is called duobinary SQPSK. The performance, characterized by P_e as a function of the receiver input E_b/N_o, of duobinary SQPSK at 3 bps/Hz is only slightly degraded from conventional SQPSK at 2 bps/Hz. Hence, duobinary SQPSK has the capability to increase bandwidth utilization by 50 percent in a linear channel. Since the adaptive equalizer compensates for the detector in forming the overall duobinary response, performance is the same with either a sampling detector or an integrate-and-dump detector.

- Duobinary SQPSK modem implementation can be based on decision-directed carrier phase tracking. Phase slips by 90° do not occur with this technique, provided that the bit synchronizer maintains the timing. This carrier tracking mechanism is closely equivalent to the LMS algorithm for controlling gain and phase of a single tap weight. A multiple-tap adaptive equalizer within the receiver simultaneously corrects phase distortion in the channel. The adaptive equalizer control in the receiver is decision-directed from the error with respect to duobinary hard decisions; that is, a soft decision v is quantized to the ternary levels

$$+1; \quad .5 < v$$
$$0; \quad -.5 < v < .5$$
$$-1; \quad v < -.5$$

of ideal duobinary.

In the simplest demodulation of duobinary, ± 1 levels denote a binary 0 for the data bit, while the 0 level denotes a binary 1 for the data bit. Maximum likelihood demodulation of duobinary by a simple two-state Viterbi algorithm (independently on I and Q for SQPSK) improves performance by 3 dB and has a greater tolerance for nonlinear distortions in the channel. Soft decision quantizing to 4 bits yields Viterbi algorithm performance close to the unquantized case.

With integrate-and-dump detection in the receiver, the desired duobinary response is closely approximated with linear-phase, maximally-flat filters. The design point is $BT_b = 0.4$, corresponding to 2.5 bps/Hz, but the data rate can be varied from 1.5 bps/Hz to 3 bps/Hz in fixed bandwidth filters.

- The Harris MD-1002 conventional SQPSK modem can, in principle, be modified to duobinary SQPSK operation using sharp-cutoff external filters. The quadrupling loop presently used for carrier tracking is discarded and replaced by a decision-directed carrier phase tracking loop and gain-control loop. The loop bandwidth can be as wide as .005 times the total bit rate without excessively degrading performance. The bit synchronizer is unmodified; however, the duobinary soft decisions are to be extracted at the bit edges (or transitions) rather than at the midpoint. For SQPSK, this is equivalent to interchanging the I and Q sampling times. The soft decisions should be quantized to 4 bits. Carrier synchronization is detected by the tendency of the soft decisions to cluster near the ternary levels of duobinary.

- A study of convolutional encoding/Viterbi decoding in combination with duobinary was made. Note that the two techniques are in conflict since redundant coding reduces the data rate, while the objective of duobinary is to increase the achievable data rate in a given bandwidth. Although rate-1/2 coding with duobinary SQPSK is found to substantially reduce the required E_b/N_o, rate-3/4 coding of conventional SQPSK offers the same bandwidth utilization and an even lower E_b/N_o. Furthermore, the rate-3/4 Viterbi decoder for conventional SQPSK is a relatively simple modification of the standard rate-1/2 Viterbi decoder, while the rate-1/2 Viterbi decoder for duobinary is a new design and considerably more complex. Rate-3/4 coding with duobinary does not have performance advantages which merit further consideration, since the decoder is extremely complex and there is only a small reduction in E_b/N_o from uncoded conventional SQPSK at the same data rate.

- For single access (TDMA) with no equalization in the receiver and integrate-and-dump detection, minimum degradation occurs with phase distortionless, maximally-flat transmit and receive filters having $BT_b = 0.4$, although degradation remains under 1.0 dB over the range $0.33 \leq BT_b \leq 0.48$. Using an 8-tap adaptive equalizer in the receiver (with tap spacing = T_b, degradation is lowered for all BT_b and remains under 1 dB from $BT_b = .32$ to $BT_b = 0.8$.

- Duobinary SQPSK is more sensitive to system phase distortion than is conventional SQPSK. Degradation is dependent not only on the peak phase shift over the data bandwidth but is a function of the type of phase distortion and the rapidity of its variation. For a given peak phase shift over the filter bandwidth, the highest degradation is produced by cosinusoidal phase distortion, with parabolic phase distortion producing the least degradation. For a given peak phase error, degradation increases for sinusoidal or cosinusoidal phase distortion as the ripple variation rate increases until a point where one cycle of ripple occurs over the (one-sided) filter bandwidth B.

- The degradation due to system phase distortion can be effectively removed by an adaptive equalizer which is under decision-directed control. Tap spacing is equal to T_b and the number of taps required must span the time delay of paired echoes produced by the phase distortion. In general, eight taps appear to be sufficient so the equalizer implementation is not of high complexity.

- AM-PM conversion produces higher deg .dation to duobinary SQPSK than to conventional SQPSK. F heavily-filtered channels, AM-PM conversion should be held below $4^o/dB$. Adaptive equalization cannot compensate for AM-PM conversion effects.

- Duobinary SQPSK suffers more degradation (≈ 2 dB) when accessing the Phase III TWT than occurs with conventional SQPSK, primarily due to the AM-PM conversion in the TWT. Degradation is higher for TDMA through the Phase III TWT than the Phase II TWT due to the higher AM-PM conversion of the former TWT, and degradation increases as BT_b decreases. In heavily-filtered channels, care should be taken to select a TWT with low AM-PM conversion in order to minimize degradation.

- For a saturating transmitter and satellite TWT, single access duobinary SQPSK operation requires filters with $BT_b = 0.4$ in the transmitter, satellite, and receiver. This condition implies TDMA with burst rates of 2.5 bps/Hz, an increase of 50% over the burst rate of 1.67 bps/Hz permitted with conventional SQPSK over the same saturating channel, at the expense of 2 to 3 bB higher degradation.

- Single-access duobinary SQPSK system performance remains relatively constant over a wide range of TWT input drive levels, whether or not the transmitter is linear or saturating. This insensitivity to drive implies that accurate uplink power control of the duobinary accesses is not necessary for TDMA operation.

- For FDMA operation, duobinary SQPSK produces less degradation than produced by conventional SQPSK for close signa' spacings; the opposite is true for large signal spacings. Therefore, the decision as to which technique to use depends on the necessity for packing signals as closely together as possible. If maximum band-

width efficiency is necessary, duobinary is the choice. For duobinary SQPSK, filters should have $BT_b = 0.333$ while for conventional SQPSK, the equalized filters should have $BT_b = 0.5$.

- For FDMA in a nonsaturating channel, duobinary SQPSK permits packing signals together as close as 0.75 times the first data null frequency. This corresponds to an overall transmission efficiency of 2.67 bps/Hz of bandwidth. With conventional SQPSK, the FDMA transmission efficiency is 1.8 bps/Hz. Thus, a 45 percent increase in bandwidth utilization is achieved for duobinary FDMA in the linear channel.

- For duobinary FDMA passed through the Phase III satellite TWT, the transmission efficiency is 2.25 bps/Hz, while for conventional SQPSK the efficiency is 1.8 bps/Hz. This implies a 25 percent bandwidth utilization increase for duobinary over conventional SQPSK.

- To achieve a level of degradation comparable to that for conventional SQPSK for FDMA, duobinary SQPSK operation requires that the TWT be operated at about a 3 dB greater output backoff. The most effective system operation occurs (for duobinary FDMA) when the Phase III TWT is operated at a backoff of between 5 and 7 dB from saturation.

- Duobinary SQPSK can be mixed with conventional SQPSK signalling in FDMA systems which access the Phase II or Phase III satellite channel.

7.2   RECOMMENDATIONS

Based on the study of duobinary data transmission, the following recommendations are made.

- Duobinary SQPSK appears to offer benefits for FDMA or TDMA systems where maximizing bandwidth utilization is of prime importance in digital data transmission, but a reasonable power utilization is also required.

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- Convolutional encoding/Viterbi decoding is not recommended for use with duobinary SQPSK. Instead, a capability for rate-3/4 coding with conventional SQPSK should be developed to improve bandwidth utilization for coded operation. Then, the attainable data rates and recommended modes in a linear channel are:

  1.1 bps/Hz for rate-1/2 conventional SQPSK

  1.6 bps/Hz for rate-3/4 conventional SQPSK

  2.0 bps/Hz for uncoded conventional SQPSK

  3.0 bps/Hz for uncoded duobinary SQPSK

- System phase distortion should be specified separately by the type of distortion rather than specifying only a peak phase error over the bandwidth.

- Since duobinary is very sensitive to AM-PM conversion, system elements, including the satellite repeater channel, should be designed to minimize this form of distortion.

- Although the Harris MD-1002 modem can be converted to duobinary operation, it is more desirable to develop a new high data rate modem tailored to duobinary reception. Such a receiver would contain a sampling detector, adaptive equalizer, optimized sync and phase tracking loops, 4-bit quantizer, Viterbi algorithm and optimized filters. Development of such a duobinary receiver is strongly recommended since efficient bandwidth utilization for both TDMA and FDMA operation is an important goal for future DSCS applications.

- Adaptive equalization should be considered for inclusion in the duobinary receiver.

APPENDIX A
CHANNEL MODELLING AND SIMULATION CONSIDERATIONS

Computer program SIMB was created to simulate the transmission of duobinary SQPSK over digital communication channels. The program permits the evaluation of system performance and parametric tradeoffs for various system configurations. The program has been written in Fortran IV with a structure having numerous subprogram modules performing various system element functions. In addition, effort has been devoted to making the program as flexible as possible so that the user can easily change parameter values or reconfigure the system by means of alphanumeric inputs while running SIMB.

The overall structure of the system modelled by SIMB is given in Figure A-1. Any combination of these system elements can be used in a given simulation run with element and system parameters designated by the user through namelist input statements. A full description of the system software, program parameters, and operational considerations is given in Appendix B.

Some features of the program are:

- Single or multiple carrier operation.

- Duobinary biphase (BPSK), quadriphase (QPSK) or staggered (SQPSK) operation.

- IF adaptive equalization in the receiver.

- Integrate-and-dump or sampling detector.

- Nonlinear amplification (TWT, hard limiter, and soft limiter with AM-PM conversion models) in transmitter and satellite.

- Multiple transmitter and receiver filtering (Butterworth, Chebyshev, and Gaussian).
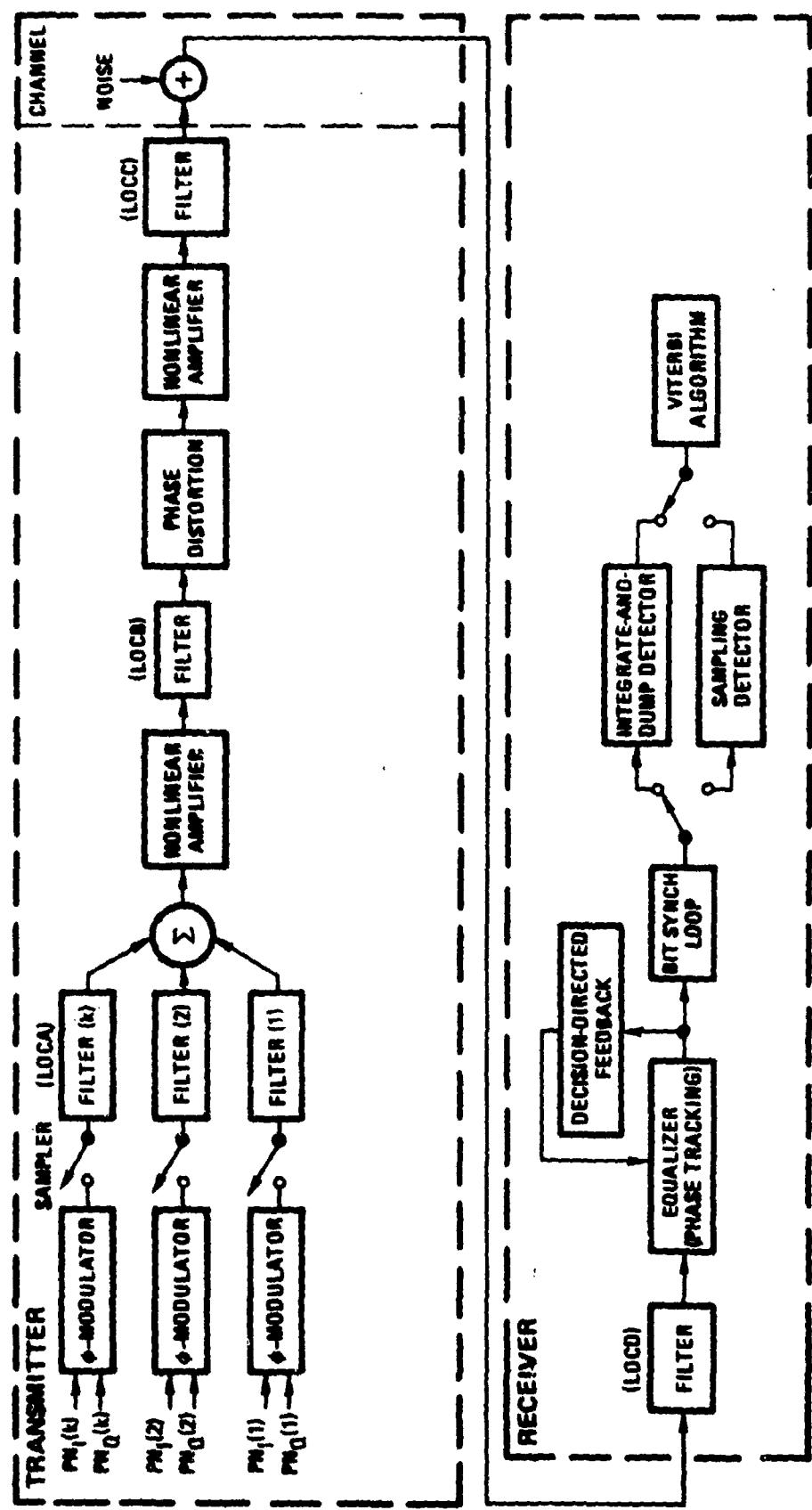
Figure A-1. Block Diagram of Overall Communication System Modelled

677-3749

- Channel phase distortion can be introduced.
- Modulator anomalies can be simulated.
- Receiver functions of automatic gain control, phase tracking, and bit synchronization are included but can be defeated.

A.1 SIMULATION TECHNICAL CONSIDERATIONS

The approach used for SIMB involves the generation of sampled-time PN (pseudonoise) sequences. These sampled time sequences are either biphase or quadriphase modulated and subsequently handled as complex baseband data, so that the arbitrary carrier frequency is suppressed in the representation. The data is handled in the time domain for the encoder, modulator, amplifiers, equalizers, detector and decoder and in the frequency domain for system filters and phase distortion elements. Conversion of the data between the time and frequency domains is performed by the Fast Fourier Transform (FFT). This section covers many of the considerations involved in the choice of program parameters for computational accuracy. These considerations include the effects of sequence length, sampling rate, Fast Fourier Transform, aliasing, and the choice of data sequences. An overall block diagram of the system simulated is given in Figure A-1.

A.1.1 SEQUENCE LENGTH

Figure A-2 depicts a binary signal extending from t_o to $t_o + \Delta t$. The duration of this signal is Δt. In the frequency domain this signal is expressed by,

$$F(f) = \int_{t_o}^{t_o + \Delta t} e^{-j\omega t} \, dt = e^{-j\omega t_o - j\omega \Delta t/2} \, \Delta t \, \text{sinc} \, (\Delta \omega t/2) , \qquad (1)$$

where $\text{sinc} \, x = \dfrac{\sin x}{x}$.

Similarly a binary message consisting of N bits becomes,

$$F(f) = \Delta t \, \text{sinc} \, (\omega \Delta t/2) \, e^{-j\omega t_o} \sum_{i=1}^{N} (-1)^{k_i} e^{-j\omega(i-1/2)\Delta t} \qquad (2)$$

where $(-1)^{k_i}$ is the polarity of the ith bit with
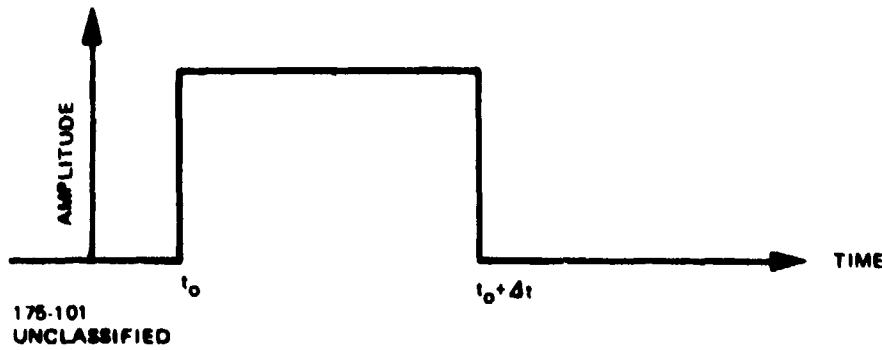
Figure A-2. Time Representation of a Binary Signal Bit

$$k_i = 0 \text{ for positive bits}$$

$$= 1 \text{ for negative bits}$$

(3)

and the first signal is assumed to originate at t_o.

The absolute value of the function, sinc $(\omega \Delta t/2)$, is represented by Figure A-3. For convenience of subsequent references $|\text{sinc}(x)|$ is also shown in the same figure. The nth null of this function occurs at $x = \pm n\pi$. Since $x = 2\pi f \Delta t/2$, the nth null also occurs at $f = n/\Delta t$.
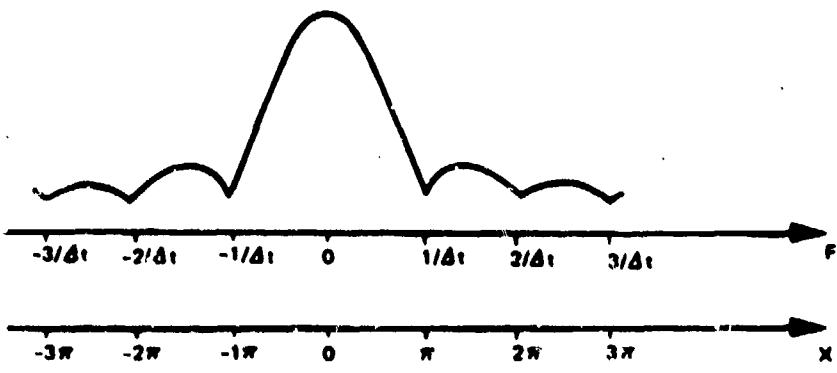
Figure A-3. $|\text{Sinc } (\omega \Delta t/2)|$ and $|\text{sinc } (x)|$ Functions

A-4

For the sake of simplicity, but without loss of generality, henceforth t_0 appearing in (1) and (2) is set to zero. Observe from (1) and (2) that the frequency spectrum is continuous. An infinite number of sample points are needed to describe a nonperiodic infinite length signal. Such signals are not well suited for computational analysis.

From the theory of Fourier Transforms, when a periodic waveform (with period T_b) is represented by a baseband signal, the spectral density of this signal can be nonzero only at $f = \pm n/T_b$; $n = 0, 1, 2, \ldots$, as shown in Figure A-4. A periodic waveform is best suited for analysis by a digital computer.

A.1.2   INPUT DATA SEQUENCES

SIMB approximates an infinite length digital sequence by repeating periodic sequences. The number of bits that constitute the periodic sequence is called the "sequence length". The time waveform is oversampled and the time between success-ive samples is called the "sampling time".

The computer simulation requires data patterns of sufficient length to allow for the occurrence of all significant intersymbol interference patterns with the relative frequency expected for independent bit streams. A maximal length shift register ("pseudonoise" or "PN") sequence has this property. Using a PN sequence of length 2^N-1 bits, the sequence taken periodically contains all 2^N-1 possible bit patterns of length N in equal frequency. If independent adjacent quadriphase channel sequences are required, a different PN sequence can be used for that channel or the same sequence can be used in a shifted version.

These sequences optimally account for intersymbol interference within their prescribed length constraint and larger sequence lengths more accurately pre-dict intersymbol interference effects as filter bandwidths become narrow compared to the bit rate. Use of the PN sequence and the discrete Fourier transform in the simula-tion eliminates bothersome "end effects" since all computations are performed modulo the sequence length.

SIMB has provisions for delaying the Q (quadriphase) channel PN sequence with respect to the I (in-phase) channel sequence. With the delay, intersymbol inter-ference patterns generated at the end of the block loop back to the beginning so that all data bit patterns in the Q channel still have equal weight. Staggered quadriphase (SQPSK) can also be simulated by delaying the Q data one half bit time from the I data.
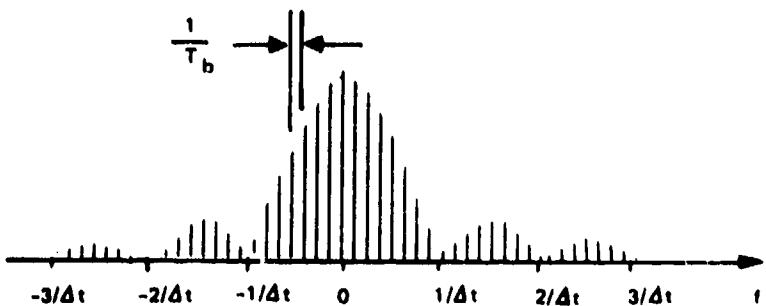
Figure A-4. Nonzero Frequency Values are Separated By
The Inverse of Time Period, T_b

KEY:

FREQUENCY RANGE OF
NON-ZERO FREQUENCY
COMPONENTS

RATIO OF SAMPLING
RATE TO BIT RATE

2

4

6
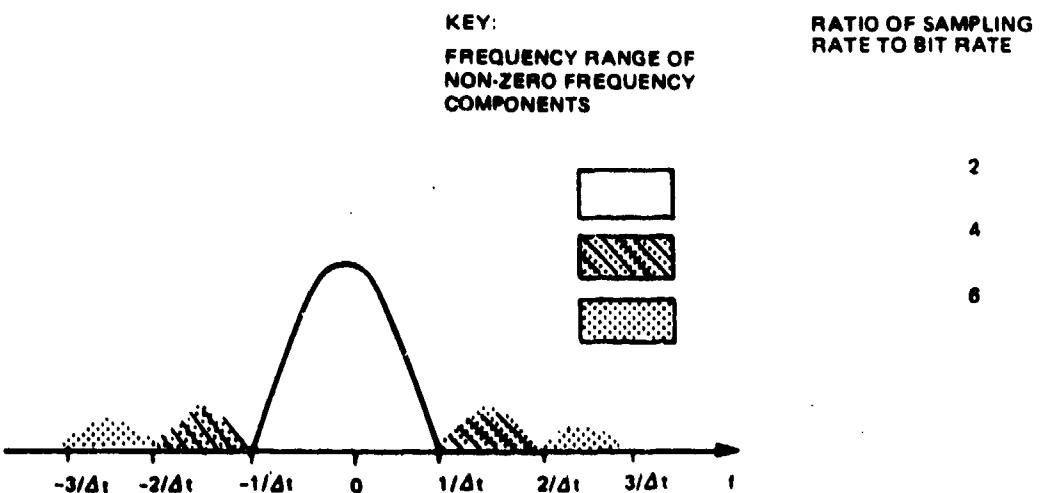
Figure A-5. Effect of Sampling Rate on Signal Distortion

The selected PN sequences are sampled at equidistant points with the total number of samples = NSMP, the sampling value specified by the user. With a 32 length sequence and 1024 samples, each bit is sampled 32 times. The sampling time interval τ is determined by the bit rate BR and, in the above case is

$$\tau = 32/(1024 \times BR)$$

The user specifies the bit rate BR (or as an alternative the bit time TBD = 1/BR) and all system bandwidths must be entered relative to this bit rate.

The above assumes a constant sampling rate with the number of samples per sequence increasing proportionally to the increase in sequence length. This increase obviously entails a corresponding increase in computer execution time and storage.

A.1.3   SAMPLING RATE

The fundamental theorem of sampling theory states, "if a time function F (t) contains no frequency components higher than F cps, then the time function can be completely determined by specifying its ordinates at a series of points spaced every 1/2F seconds or less." When nonzero frequency components occupy the entire spectrum from 0 to F, then the minimum required sampling rate to prevent distortion is 1/2F. It follows then that sampling a baseband signal at a rate 1/2F will neglect all frequency components above F.

In the present context sampling rate refers to a numerical evaluation process. To transform the signal from time to frequency domain, the computer takes s time samples per bit; s being the sampling rate normalized with respect to bit rate. Figure A-5 illustrates the "filtering" effect of finite sampling rate. Sampling at twice the bit rate (s=2) has the effect of "ideal" first null filtering. All frequency components outside the darkened area are set to zero due to insufficient sampling rate. As the sampling rate increases, the resulting spectrum more closely approximates the actual unfiltered spectrum. Sampling at 6 times the bit rate eliminates the spectra only past the third null.

The required sampling rate (relative to the bit rate) is determined by the kind of filtering performed in the transmission link, and by the non-linear amplifiers following these filters. Non-linear amplifiers usually generate intermodulation products; hence they "spread" the signal spectrum in frequency domain. This spreading, not the computational errors, determines the spectral occupancy of the signal.

The numerical sampling used to perform the conventional Fourier Transform has the effect of an ideal bandpass filter. The "filter" cut-off frequency is at $\pm(s\Delta t/2)$. s (not necessarily an integer) is the average number of computational time samples per bit duration Δt. Throughout, a uniform sampling rate is assumed. Since the "filter" is ideal, no signal distortion occurs at frequencies below cut-off. Actually, the present program employs Fast Fourier Transformation (FFT). It is shown below that the FFT does have the same cut-off characteristics as the conventional FT, but also introduces approximation errors at frequencies below cut-off.

A.1.4   FAST FOURIER TRANSFORMATION (FFT)

As implied by its name, the FFT saves significant computer time over conventional Fourier Transformation. This saving does not come freely. Above, it was shown that insufficient sampling rate results in non-ideal filtering when conventional Fourier Transformation is used for signal conversions between time and frequency domains. It will be shown that the FFT introduces additional errors due to "aliasing".

The mathematical treatment of the discrete Fourier transform follows, where Δt is the sampling time spacing, Δf is the sampling frequency spacing, N is the number of sample points used, and $x(m\Delta t)$ is the mth data sample.

$$x(m\Delta t) = \sum_{n=\frac{-N}{2}+1}^{N/2} X(n\Delta\omega)\,\Delta f e^{jnm\Delta\omega\Delta t} \tag{4}$$

choose $\Delta\omega$ and Δt so that $\Delta\omega\Delta t = 2\pi/N$:

$$x(m\Delta t) = \sum_{\frac{-N}{2}+1}^{N/2} X(n\Delta\omega)\,\Delta f e^{jnm\frac{2\pi}{N}} \tag{5}$$

$$= \sum_{0}^{N/2} X(n\Delta\omega)\,\Delta f e^{jnm\,2\pi/N}$$

$$+ \sum_{\frac{N}{2}+1}^{N-1} X((n-N)\Delta\omega)\,\Delta f e^{j(n-N)m\frac{2\pi}{N}} \tag{6}$$

Then $-Nm \frac{2\pi}{N}$ can be dropped in the second exponent by periodicity. Let

$$X_m \;\; \cdots \;\; x(m\Delta t) \tag{7}$$

and use the following notation for the transformed quantities:

$$X_n = \begin{cases} X(n\Delta\omega)\,\Delta f & , \quad 0 \le n \le \frac{N}{2} \\[2ex] X((n-N)\Delta\omega)\,\Delta f & , \quad \frac{N}{2}+1 \le n \le N-1 \end{cases} \tag{8}$$

etc. This is equivalent to taking the negative frequency portion of the transformed values and shifting it upward by $N\Delta\omega$. Then:

$$X_m = \sum_{n=0}^{N-1} X_n \, e^{jnm\frac{2\pi}{N}} \tag{9}$$

This is just the discrete Fourier (inverse) transform and can be evaluated rapidly by the Fast Fourier transform algorithm. Including the forward and inverse transforms, computations proportional to NlogN are required. For N samples in the time domain, computations proportional to N^2 are required. Except for very simple filter structures, the constant of proportionality to N is greater for the all-time domain method than the constant of proportionality times log N for the Fourier transform method. (Note that it is desirable to make the block size N as small as possible for a given number of bits, M, to reduce the log N factor.) For a given data bit sequence of length M, there are N/M samples per bit.

The discrete Fourier transform is periodic in the sense that

$$X_{m+N} \;\; = \;\; X_m \tag{10}$$

Although one is really only interested in X_m for m = 0, 1, ..., N-1, the importance of this property is that end effects are eliminated and intersymbol interference patterns generated at the end of the block loop back to the beginning. The net effect (for N reasonably large compared to the filter time constant) is that of a system where the same data sequence is sent over and over again.

The FFT produces a repetitive frequency spectra. The frequency separation between these spectra is equal to the number of samples per bit divided by the bit time. As shown by Figure A-3, the nth null of the sinc $(w\Delta t/2)$ spectrum occurs at $f = n/\Delta t$; Δt being the bit duration. (Throughout, baseband signals are assumed.)

Hence, the number of computational time samples per second determines the aliasing frequency. Equivalently, the number of samples per bit duration, s, determines the aliasing frequency normalized with respect to the first null of the frequency spectrum.

The "aliasing" phenomenon is illustrated in Figure A-6. Figure A-6A shows a finite bandwidth spectrum with cut-off frequency, $f_{c.o.} \simeq \pm 2.7/\Delta t$. When the time domain equivalent of this spectrum is converted to the frequency domain using conventional Fourier Transform on a digital computer, Figure A-6B results. Figure A-6B assumes that the computer calculates the frequency response by sampling the time function at a uniform rate, $s = 3$. Figure A-6C displays the resulting spectrum when the FFT computer routine is used instead of the regular Fourier transform routine. Because FFT introduces repetitive frequency spectra, the tails of the adjacent (erroneous) spectra fall into the actual signal spectrum introducing computational errors. As shown by Figure A-6D the FFT truncates the frequency spectrum to a signal period of the repetitive sequence, but only after introducing aliasing errors due to spillover from physically nonexistent spectra; that is, from spectra that only exist for computational ease.

Parameter s gives the total frequency range covered in the simulation if bit rate is unity. As an example, if NSMP = 512 and LSEQ = 31, $s = \frac{512}{31} \simeq 16$ Hz. Since the bandwidth is two-sided this represents the frequency range [-8 Hz, 8 Hz]. For a non-unity bit rate, BR, the frequency range covered equals $s \cdot BR$. Spectral energy lying outside the range $[-\frac{s \cdot BR}{2}, \frac{s \cdot BR}{2}]$ is aliased back and added to the true value to produce computational errors. For example, energy at frequency $s \cdot BR$ aliases to appear at frequency f=0. In a linear system the aliasing is minimal since the spectral energy of the PN data falls off relatively fast and system filter bandwidths further minimize the out of band response.
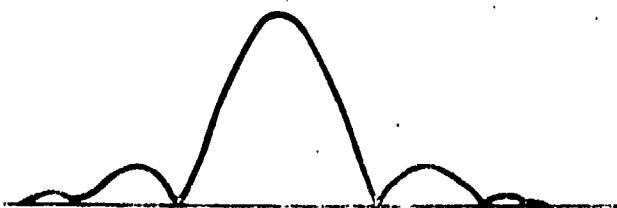
Figure A-6A. Filtered Signal Spectrum

A-10
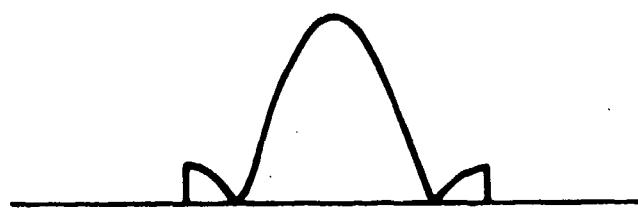
Figure A-6B. Filtered Signal Spectrum After Computational
Fourier Transform, S = 3
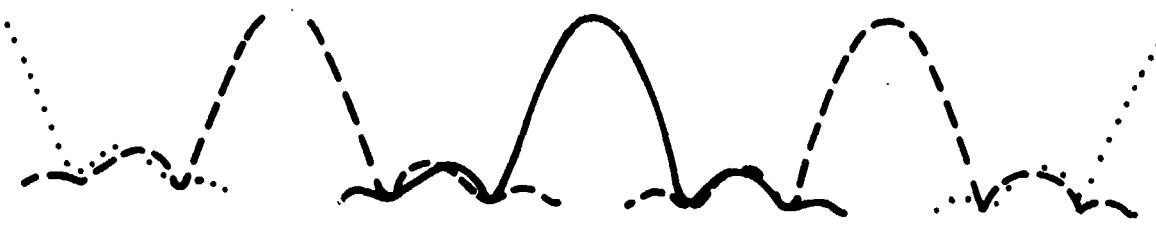
Figure A-6C. Filtered Signal Spectrum in FFT Representation,
Sampling Rate S = 3

COMPUTATIONAL ERROR
CAUSED BY "ALIASING"

Figure A-6D. Filtered Signal Spectrum After Computational
FFT, S = 3

Figure A-6. Generation of Aliasing Error in FFT

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A.2   CHANNEL ELEMENT MODELS

This section details the methods used for simulating the various system elements used in the channel. Models are given, including the technical considerations involved in the selection of these models and their parameters.

A.2.1   SIGNAL GENERATION AND MODULATION

This section details the manner in which the input data sequences to the in-phase (I) and quadrature (Q) channels of a given signal are generated, sampled, and phase modulated. In addition, the technique for generating multiple accessing signals is discussed. The following parameters and arrays used in SIMB govern the signal generation and format of the signals.

Parameter		Description
NSMP	–	The number of total signal samples used in the simulation
LSEQ	–	The length of the PN sequences generated for both the I and Q data channels
NSB	–	The number of samples per bit used (NSB = NSMP/LSEQ)
QDEL	–	The relative delay between bits in the I and Q channels (given in fraction of a bit)
MPSK	–	The type of phase modulation used (=2) biphase (=4) quadriphase (QPSK) or staggered quadriphase (SQPSK)
ISQ	–	Indicates whether QPSK or SQPSK (=0) QPSK (=1) SQPSK – implies QDEL = .5
G(4)	–	Four values of modulator gain
P(4)	–	Four values of modulator phase locations (nominally 0°, 90°, 180°, 270°)
NCHAN	–	Number of accessing signals in the communications channel
Z(NSMP)	–	Array of the NSMP complex signal samples
FCENT	–	Specifies center frequency offset (normalized by the bit rate) of the accessing signals
CPR(NCHAN)	–	Specifies power in each accessing signal

A.2.2 GENERATION OF PN SEQUENCES

Subroutine XCOD is used to generate the PN data sequences required. Function MSRG is a function subprogram which simulates a modular shift register binary code generator. XCOD generates an initial state for the shift register and the feedback tap vector ITAP to generate a maximal length sequence of LSEQ bits and than calls MSRG for the I and Q channels. Care is taken to insure that different PN sequences are used for the I and Q channels to eliminate performance anomalies that could result from correlation effects if the same sequences were used. The PN sequences are returned in arrays RI and RQ. Arrays RI and RQ replace the sequence of 0 and 1 values by the values −1 and +1 for modulation.

A.2.3 SIGNAL SAMPLING

The LSEQ bit values in arrays RI and RQ are time-sampled to NSB samples per bit and then stored in the array Z of dimension NSMP. If shifting parameter QDEL is not zero, the sampling of the Q channel is delayed by QDEL · NSB samples. For SQPSK, the sampling of the Q channel is delayed by NSB/2 samples.

A.2.4 PHASE MODULATION

The sampled-time data sequences are input to a modulator (subroutine CMOD) which can be user-specified as biphase or quadriphase. For quadriphase, different PN sequences are used in the in-phase and quadrature channels. The modulator outputs are

$$\alpha_1 e^{j\beta_1}$$
$$\alpha_2 e^{j(\frac{\pi}{2} + \beta_2)}$$
$$\alpha_3 e^{j(\pi + \beta_3)}$$
$$\alpha_4 e^{j(\frac{\pi}{2} + \beta_4)}$$

(11)

In the default mode (ideal modulator), $\alpha_1 = \alpha_2 = \alpha_3 = \alpha_4 = 1$ and $\beta_1 = \beta_2 = \beta_3 = \beta_4 = 0$. For biphase operation, $\alpha_2 = \alpha_4 = 0$. To simulate the effects of modulator phase and amplitude imbalance, the user can input new values of the α and β parameters through namelist INPT parameters G and P.

Each time-sample of the I and Q data sequences is scaled in amplitude and shifted in phase, as required, to permit the evaluation of channel crosstalk and performance degradation as a function of modulator anomalies. In a communications system, the data modulates an RF carrier. In SIMB, the carrier is assumed to be at a frequency very much larger than the bit rate. Therefore, the center channel data samples are handled as complex quantities at baseband in the simulation. If several carriers are simultaneously accessing the channel, modulation is treated as described in Section A.2.5.

A.2.5   MULTIPLE ACCESSING CARRIERS

The previous sections have assumed the case of a single phase-modulated carrier passing through the communications system. A typical channel may have multiple signals passing through the channel producing various effects such as AM-PM conversion, signal suppression, and adjacent channel interference. SIMB allows such multiple carrier operation. Most system elements presented in this report operate in the same manner regardless of the number of signals present. The main exception involves changes in the signal generation/modulation section of the program.

With multiple carrier operation, the user inputs the number of carriers desired, NCHAN. The desired composite signal structure is set up subject to the limitation that all carriers have the same phase modulation (BPSK, QPSK, or SQPSK). A loop is formed within SIMB which sequentially performs the following operations for each carrier.

a.   PN sequences are generated for the I and Q components of that carrier. Care is taken to insure that all PN sequences generated for the various carriers are different.

b.   These sequences are appropriately sampled and phase modulated in the time domain to form an array of NSMP complex time samples of that carrier at baseband. The bit transition times of the sequences are offset by one-eighth of a bit duration to randomize the composite waveform.

c.   This array of time samples is converted to the frequency domain via the FFT and filtered (if desired) by a filter structure input by the user.

d.   These (filtered) frequency samples are then shifted in the frequency domain to form a signal offset in frequency from baseband by an amount FCENT specified by the user. FCENT is the center frequency of that signal normalized by the bit rate.

e.   The (shifted) frequency samples are converted to the time domain by the FFT, scaled by the amplitude $\sqrt{CPR}$ specified for that channel, and added to the NSMP time samples already generated for the other carriers.

Operations (a) through (e) are performed for each of the NCHAN carriers so that the final array of time samples contains the composite waveform resulting from the multiple carriers desired. Note that the channel on which detection is performed must be specified as baseband; i.e., no frequency offset. If convolutional encoding is desired by the user, it is performed on that channel specified as baseband.

The composite array of time samples are sequentially passed through the various system elements as for the case of a single carrier. Detection and decoding are performed for only the baseband signal. Operational considerations for multiple carrier operation are given in Appendix B.

One limitation concerns the permissible location of signals which are off-set in frequency from the center channel. As an example, consider NSMP = 1024 time samples, and NSB = 32 time samples per bit. The total frequency range covered is from -16 to +16 times the bit rate. Spectral energy lying outside this frequency band is aliased to give erroneous results within the specified frequency range. Although the data spectrum falls off rapidly after the first few nulls, if an adjacent channel is displaced further than about 8 nulls (FCENT = ±8) from the center channel, aliasing could become a problem. System filters help to alleviate the magnitude of such aliasing in the desired signal spectrum, however, and placement of adjacent channels

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further than 8 nulls from the desired channel is not necessary in system scenarios investigated.

A. 2. 6   FILTERS

Filters can be inserted at four separate system locations within the structure of SIMB. These locations are user-specified as LOCA, LOCB, LOCC, and LOCD (see Figure A-1). Any combination of these four locations can be input in a given run and the various filters can be of different types with differing parameters.

Filtering is performed in the frequency domain. The sequence of signal time samples Z is transformed to frequency domain samples via the Fast Fourier Transform (FFT) and multiplied by the corresponding filter frequency response samples. This operation is performed in subroutine FDOM.

Three ideal filter types can be simulated within SIMB; Butterworth, Chebyshev, and Gaussian filters. In addition, phase distortionless filters with a maximally-flat amplitude characteristic are modelled in the frequency domain. The appropriate filter type and appropriate filter parameters are inserted by the operator through namelist FLTR. Subroutine PPIN computes and stores the ideal filter pole locations. These pole locations are computed for an ideal filter of the type specified with bandwidth normalized to 2π radians.

While the modulator output data can be easily filtered in the time domain, the effects of other system filters are simulated in the frequency domain to avoid the lengthy computations that would be required to convolve the digital data samples with the filter impulse response. The input data to the filter is converted to the frequency domain through use of the Fast Fourier Transform and these complex frequency samples are multiplied by the corresponding frequency response samples of the filter as obtained by calls to subroutine FFR.

Care must be taken when transforming between the time and frequency domains to prevent aliasing errors due to replication by the FFT. Such errors are negligible in the current simulation since the sampling intervals have been chosen to cover a sufficiently wide bandwidth so that such aliasing terms are very low at band edge. Therefore, virtually the same results are obtained whether the filtering is performed in the frequency or in the time domains.

The pole locations of the various ideal filters are computed as follows (for unity bandwidth):

Butterworth Filters

The analytical form of a Butterworth filter is

$$|F(j\omega)|^2 = 1/(1 + \omega^{2n}) \tag{12}$$

The poles are uniformly distributed on the unit circle in the left half plane and the n pole locations are

$$p_k = \exp\{j(2k-1+n)\pi/2n\}, \quad k=1, 2, \ldots, n \tag{13}$$

Chebyshev Filters

The analytical form of a Chebyshev filter is

$$|F(j\omega)|^2 = 1/[1+\delta^2 T_n^2(\omega)] \tag{14}$$

when δ specifies the ripple amplitude and $T_n(\omega)$ is a Chebyshev polynomial given by

$$T_n(\omega) = \cos(n \cos^{-1}\omega) \text{ for } |\omega| \leq 1 \tag{15}$$

Designating the n poles by $P_k = \sigma_k + j\omega_k$, we get

$$\sigma_k = \sinh\left(\frac{1}{n} \sinh^{-1}\frac{1}{\delta}\right) \sin\frac{2k-1}{n} \frac{\pi}{2} \tag{16}$$

$$\omega_k = \cosh\left(\frac{1}{n} \sinh^{-1}\frac{1}{\delta}\right) \cos\frac{2k-1}{n} \frac{\pi}{2} \tag{17}$$

for $k = 1, 2, \ldots, 2n$, taking only those poles in the left half plane. Another interpretation of these expressions can be obtained by squaring both sides, adding, and dividing by the hyperbolic function to yield

$$\frac{\sigma_k^2}{\sinh^2\left(\frac{1}{n} \sinh^{-1}\frac{1}{\delta}\right)} + \frac{\omega_k^2}{\cosh^2\left(\frac{1}{n} \sinh^{-1}\frac{1}{\delta}\right)} = 1 \tag{18}$$

This is the equation of an ellipse in the s-plane with the major axis lying along the $j\omega$ axis.

Gaussian Filter

The Gaussian power density spectrum is

$$|F(j\omega)|^2 = \exp\left(-\frac{1}{2}(2\ln 2)\omega^2\right) \tag{19}$$

In the frequency domain, equation (19) could be used directly.*

No convenient expression exists for analytically determining the poles of a Gaussian filter so a 3-pole low-pass filter was numerically optimized to synthesize a Gaussian response. Starting with a 3-pole Bessel filter of unity bandwidth, a conjugate-gradient optimization program was used to vary the pole locations so as to most closely approximate a Gaussian filter over the range of ω_c [-3, 3]. The resulting 3-pole filter has poles at

$$p_1 = -a, \quad p_2 = -b + j\omega_1, \quad p_3 = b - j\omega_1$$

where $a = 1.02437$, $b = .956519$, and $\omega_1 = 1.17703$.

Phase-Distortionless Maximally-Flat Filters

A five-pole filter having a maximally-flat amplitude response with zero phase shift simulates a transversal filter response such as that obtained with surface wave devices at IF. This filter is simulated in the frequency domain by first converting the time samples Z to the frequency domain and multiplying the frequency samples by the corresponding filter response in subroutine FDOM. The response of this filter is given in the frequency domain as

$$|F(j\omega)|^2 = 1/[1 + (\omega/\omega_c)^{10}]$$

$$\angle F(j\omega) = 0 \tag{20}$$

where ω_c is the 3-dB filter bandwidth

A.3 NONLINEAR AMPLIFIER

Subroutine AMP models several user-selected nonlinear amplifiers in the time domain. Soft limiters, hard limiters, and two travelling wave tube (TWT) amplitude characteristics are modelled as are four different amplifier phase characteristics. Input signal time samples are phase shifted and scaled in magnitude in accordance with the amplitude and phase types selected and amplifier parameters input by the user. The various amplifier models are described in this section. Any combination of phase and amplitude types is permitted.

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*For compatability with generation of the other filter responses and to facilitate generation of step and ramp responses, the filter is computed from stored pole locations.

A.3.1 AMPLIFIER AMPLITUDE CHARACTERISTICS

A.3.1.1 Hard Limiter

Input TYPE = 3 models the ideal hard limiter producing the saturated amplifier output independent of gain. The transfer function of the hard limiter is given by

$$Z_o = V_{sat} \cdot Z_i / |Z_i| \tag{21}$$

where Z_i is the complex input time sample, Z_o is the complex output time sample, and V_{sat} is the saturated output voltage.

A.3.1.2 Soft Limiter

The soft limiter model (TYPE = 2) assumes a piecewise linear amplifier which has linear amplification until the input signal amplitude exceeds a prescribed level above which hard limiting occurs. The soft limiter model is described by the equations

$$Z_o = \begin{cases} V_{sat} \cdot GI \cdot Z_i/\sqrt{.1} \,, & |GI \cdot Z|^2 \le .1 \\ V_{sat} \cdot Z_i/|Z_i| & , & |GI \cdot Z|^2 > .1 \end{cases} \tag{22}$$

where GI is the amplifier gain in the linear region.

A.3.1.3 Traveling Wave Tube (TWT) Models

The primary nonlinear device in a satellite is usually a TWT (TYPE = 1, 4, or 5) used for the high level power amplification. This amplifier exhibits both nonlinear amplification and a linear or nonlinear phase shift. Furthermore, military repeaters usually contain a tunnel diode amplifier limiter (TDAL) or other limiter which controls the characteristics of the repeater in the region of saturation.

The TWT amplifier models are a function of the complex input waveform $Z_i(t)$. The power of this input waveform is P_i. At the input of the amplifier any signal power loss resulting from filtering is removed by normalizing the input power (over the NSMP samples) to unity through a call to AGC. The amplifier operating point is then calculated based upon the output backoff (BO, in dB) entered by the user. TWT backoff is defined as

$$BO = P_o/P_{sat} \tag{23}$$

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where P_{sat} is the saturated TWT output power at BO $\cdot$ 0 dB and P_o is the backed-off amplifier output power for a normalized amplifier input power of unity.

A.3.1.4   TWT Amplifier Model (TYPE = 1)

The amplifier gain GI is specified indirectly to produce an amplifier output power P_o for $P_1 = 1$, following user specification of the backoff value BO. The amplifier gain GI is a nonlinear function of P_1, P_o, and BO. The gain GI is found by a search procedure to minimize the expression

$$|Z_o - V_o| \text{ for } Z_1 = 1 \tag{24}$$

where

$$V_o = (GI \cdot V_1) = \begin{cases} 1, & |GI \cdot V_1| \le C \\ \dfrac{10^Y}{GI \cdot V_1}, & |GI \cdot V_1| > C \end{cases} \tag{25}$$

$$Y = A \cos [\log_{10} (GI \cdot V_1/D)/B] - A \tag{26}$$

Parameters A, B, C, and D are dependent on the assumed TWT amplifier characteristic. The values used for a general TWT characteristic are:

$$A = 0.3935$$
$$B = 0.4753$$
$$C = 0.3548$$
$$D = 2.317$$

These parameters give the characteristic shown in Figure A-7.

Prior to operation of the subroutine AMP, gain GI is determined by a search procedure so that the amplifier is operating at the correct backoff specified by the user. Following selection of the proper gain GI, input time samples are appropriately amplitude scaled by the equation:

$$Z_o = \begin{cases} V_{sat} \cdot GI \cdot Z_1 & , |GI \cdot Z_1| \le C \\ V_{sat} \cdot Z_1 \cdot 10^Y /|Z_1| & , |GI \cdot Z_1| > C \end{cases} \tag{27}$$

where Y is given by equation (26) and A, B, C, and D are the constants previously given.
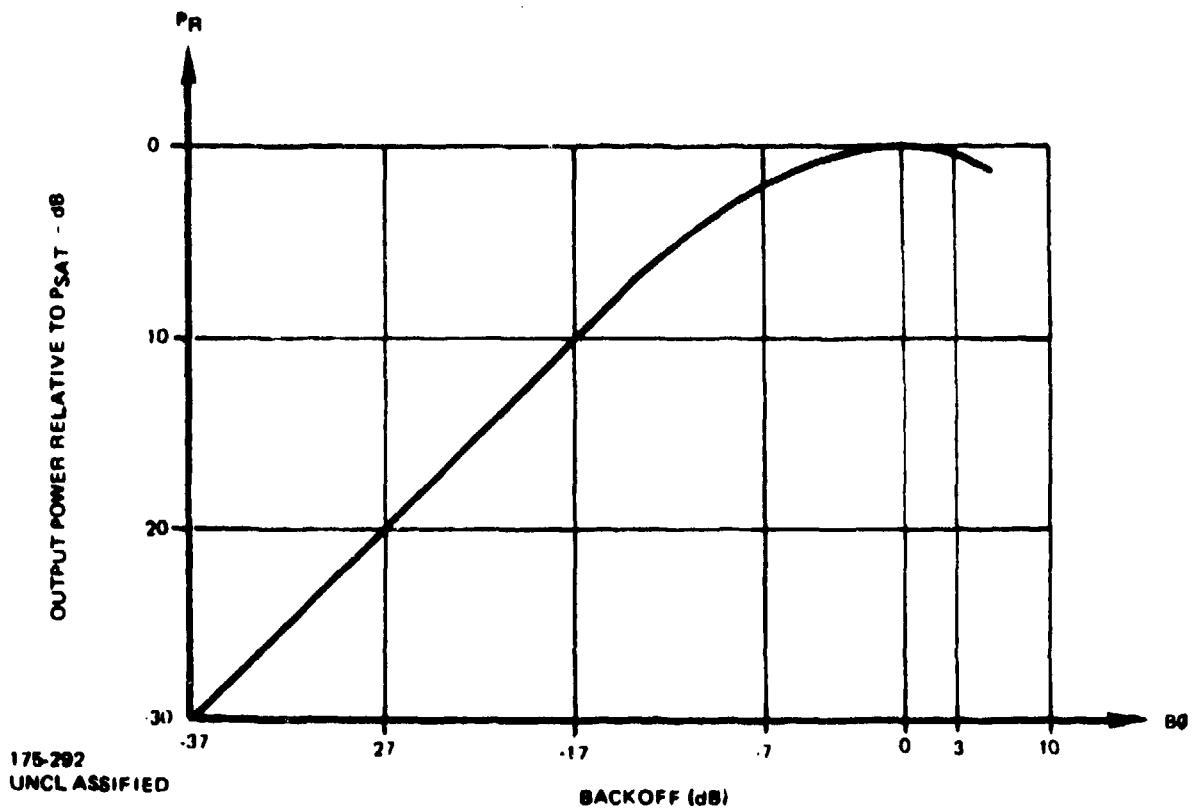
Figure A-7. Generalized TWT Gain Characteristic Modelled when TYPE = 1

A.3.1.5 Hughes' TWT Model (TYPE = 4)

The amplitude characteristic of the Hughes' TWT for Phase III operation
is shown in Figure A-8 and is modelled in AMP by specification of the input/output
values at 5 dB increments over the range of -20 dB $<$ BO $<$ 0 dB. Linear interpolation
is used for values between specified points. For BO $<$ -20 dB, linear gain is used.
For BO $>$ 0 dB, the amplitude is hard limited to the 0 dB level. Also, the phase shift
is held constant for BO $>$ 2 dB.

As noted above, a military repeater will have a limiter, and the gain
budget will normally limit the input drive to the TWT such that its maximum output
is near the saturation point. Thus, the characteristic is correctly modelled for
BO $<$ 0 dB and is a typical representation for BO $>$ 0 dB.

A-21
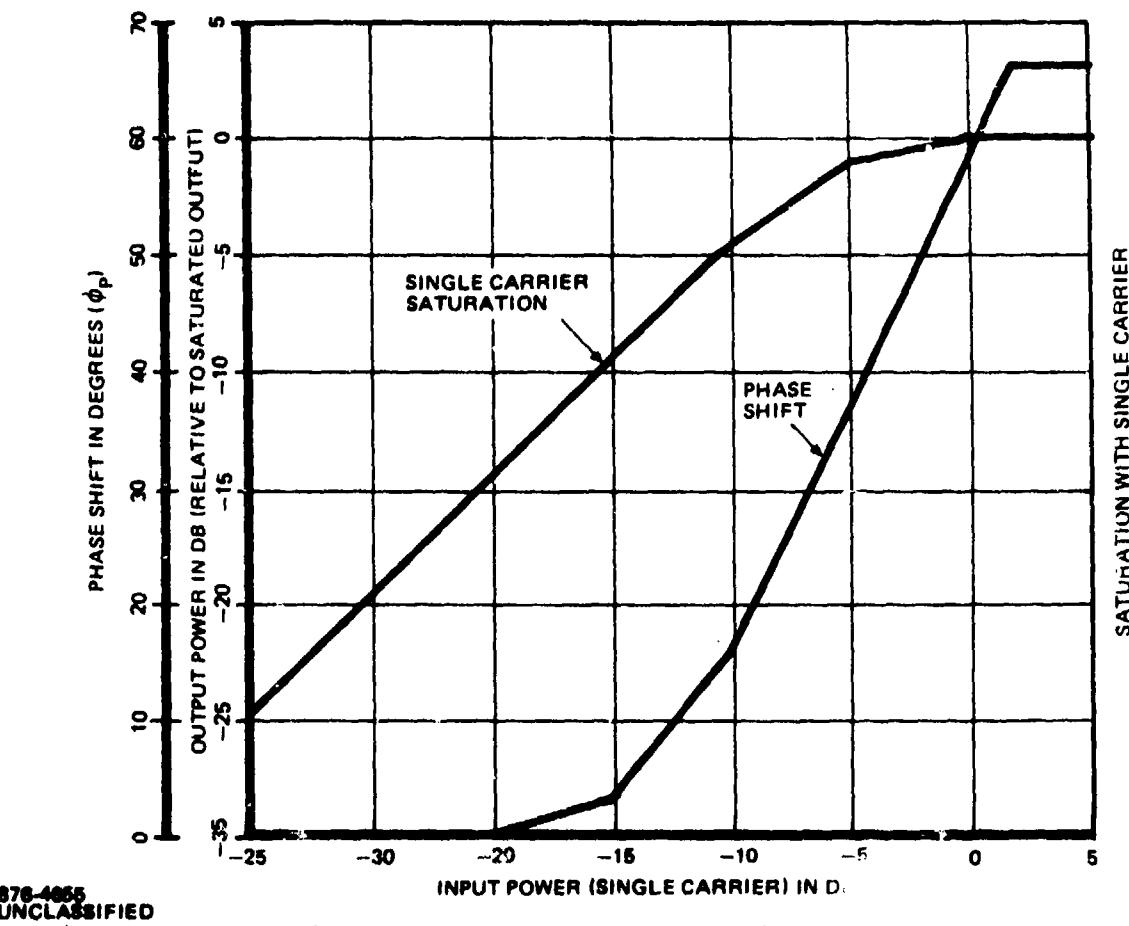
Figure A-8. Amplitude and Phase Characteristic of the Hughes' TWT

A.3.1.6   Phase II TWT Model (TYPE = 5)

The amplitude characteristic of the Phase II TWT is shown in Figure A-8 and is modelled in AMP by specification of the input/output values at 5 dB increments over the range of -15 dB < BO < 0 dB. Linear interpolation is used for values between specified points. For BO < -15 dB, a linear gain is used. For BO > 0 dB, the amplitude is hard limited to the 0 dB level.
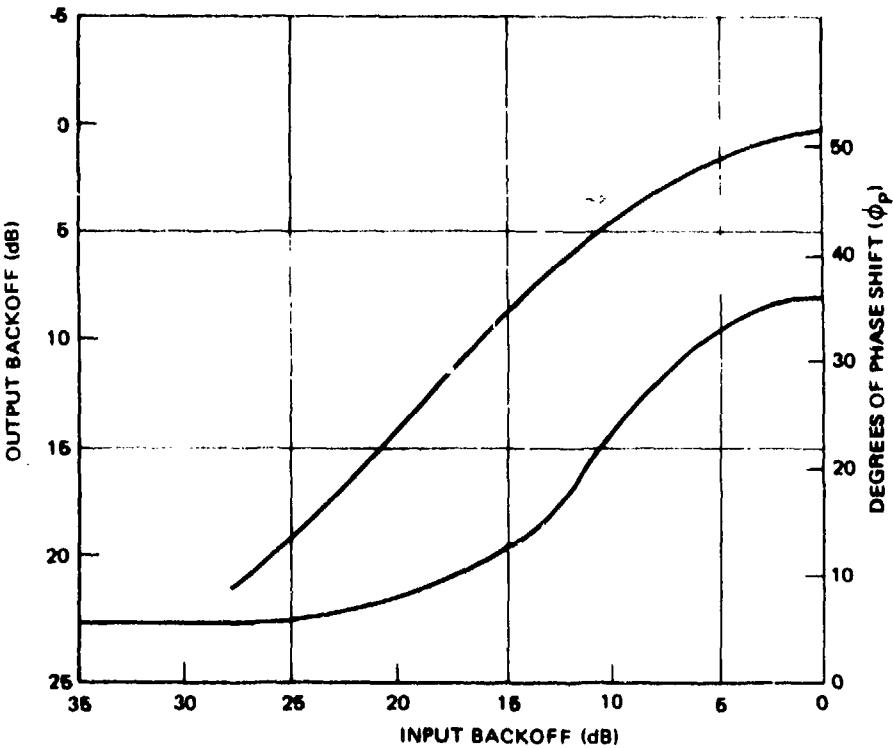
Figure A-9.   Amplitude and Phase Shift Characteristics of Phase II TWT

A.3.2   AMPLIFIER PHASE CHARACTERISTICS

Four amplifier phase characteristics are available. The phase models are independent of the amplitude model selected and phase rotation of each input signal sample follows amplitude scaling of the sample in subroutine AMP. If PHASE = 0, no phase rotation occurs. In all other models, the phase shift ω_p is a function of the phase characteristic selected and the amplitude of the input sample. The output sample from subroutine AMP is therefore

$$\hat{z}_o = z_o e^{j\omega_p} \tag{28}$$

The AM-PM conversion produced by the amplifier phase shift produces intermodulation effects which degrade system performance.

A.3.2.1 Berman-Mahle Model (PHASE = 1)

$$\omega_p = a(1 - \exp(-b)|GI \cdot Z_i|^2) + |GI \cdot Z_i|^2/C \tag{29}$$

where a, b, and c have the values

$$a = 0.602$$
$$b = 0.660$$
$$c = 102.4$$

A.3.2.2 Linear Phase Model (PHASE = 2)

$$\omega_p = \omega_s \cdot 20 \log_{10}(GI \cdot Z_i) \tag{30}$$

where ω_s is the specified phase shift in radians/dB.

A.3.2.3 Truncated Linear Phase Model (PHASE = 3)

The truncated linear phase is given by the expression

$$\omega_p = \begin{cases} \omega_s \cdot 20 \log_{10}(GI \cdot Z_i) \ , & GI \cdot |Z_i|^2 \geq p_f \\ \\ 0_o & , & GI \cdot |Z_i|^2 < p_f \end{cases} \tag{31}$$

where p_f is a prescribed input back-off power. At present, $p_f = 0.1$. Some TWT specifications give phase ω_s in degrees/dB while others give max phase, $\omega_{p, max}$, at BO = 0 dB. This phase characteristic is given in Figure A-10.

A.3.2.4 Hughes' TWT Phase Characteristic (PHASE = 4)

The phase shift of the Hughes' TWT as a function of drive is also shown in Figure A-8 and is modelled in AMP by specification of the phase shift versus input drive in 5 dB increments over the range -20 dB < BO < 0 dB. Linear interpolation is used for values between specified points. For BO < -20 dB, phase shift $\omega_p = 0^o$ and for BO > +2 dB, the phase shift is maintained at 66°.

$$P = G_I \cdot |Z_i|^2 \tag{32}$$

A.4   CHANNEL PHASE DISTORTION

Three types of phase distortion are modelled in SIMB. These types are sinusoidal, cosinusoidal, and parabolic phase. These phase types are shown in Figure A-10. These phase distortions are located in function DIST which returns the resulting phase φ_D at the calling frequency W. This phase is used to rotate the complex signal samples in Z which have been transformed to the frequency domain. Each type of phase distortion is described below.

A.4.1   SINUSOIDAL PHASE DISTORTION

The sinusoidal phase distortion of period T_R is given by

$$\theta(\omega) = \beta \sin(\omega T_R) \tag{33}$$

where T_R determines the ripple period in the frequency domain and the phase varies between $\pm\beta$. If T_R equals the bit period TBD, there is one ripple cycle in the first null bandwidth $[0 \leq \omega \leq 2\pi TBD^{-1}]$. Ripple frequency $FR = T_R^{-1}$.

A.4.2   COSINUSOIDAL PHASE DISTORTION

Cosinusoidal phase distortion of period T_R and amplitude β is given by

$$\theta(\omega) = \beta \cos(\omega T_R) \tag{34}$$

A.4.3   PARABOLIC PHASE DISTORTION

The assumed parabolic phase characteristic is

$$\theta = \beta \left[\frac{\omega T_R}{2\pi}\right]^2 \tag{35}$$

where β is the phase error developed at (radian) frequency $\omega = 2\pi/T_R$. This phase variation yields the time delay variation

$$\frac{d\theta}{dw} = \beta \frac{T_R^2}{2\pi^2} \omega \tag{36}$$
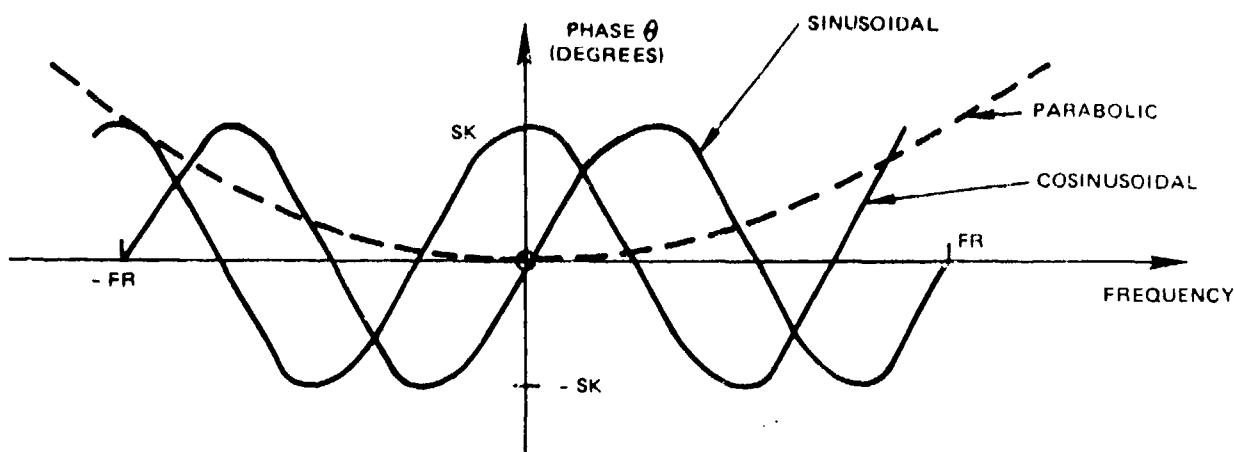
Figure A-10. Phase Characteristics Modelled

A.5 DUOBINARY RECEIVER MODEL

The basic flow of data through the receiver is illustrated in Figure A-1. The signal and noise first pass through the receiver filter and the resulting filtered noise power is computed. The filtered data is next phase tracked or adaptively equalized; if equalized, the equalizer performs the required phase tracking. Bit sync is then established and the data is demodulated using an integrate-and-dump, detector. The detected bits are passed through the Viterbi algorithm and the differentially decoded output bits are used for estimating the probability of bit errors. The individual receiver elements are described in the following sections.

Note that the equalizer/phase tracking and bit sync are embedded in a loop. The loop uses the filtered data as input and searches for the correct bit sync position, equalizing/phase tracking at each iteration of the bit sync until the process converges at the correct sync and equalizer tap weight values. The integrate-and-dump detector operates on 'he equalized data using the optimal sync obtained.

A.5.1 RECEIVER AGC

Prior to receiver filtering, an automatic gain control (AGC) loop normalizes the receiver input signal energy to unity to provide the appropriate input E_b/N_o level specified. The AGC action is performed by the expression

A-26

$$AGC = \sqrt{\left(\sum_{i=1}^{NSMP} Z_i \cdot Z_i^* \right) / NSMP}$$

where Z_i^* is the complex conjugate of the ith time sample. Subsequently, for the QPSK data each time sample is multiplied by the value $(\sqrt{2}/AGC)$.

For multiple accessing signals, the AGC value is computed and then increased by a factor β to bring the energy of the signal in which probability of error is to be computed to unity. This rescaling of amplitude relates the user-specified received E_b/N_o to the energy in this central signal. If the composite received waveform contains N adjacent signals, with the kth adjacent signal having power P_k and the center signal having power P_c, then

$$\beta = \frac{P_c + \sum_{k=1}^{N} P_k}{P_c} \qquad (37)$$

Note that NCHAN = N + 1 and the P_k are given by the values CPR entered by the user for each accessing signal. While the ratio β is strictly accurate only for linear channels, suppression effects in the normal saturating channel are minor and are not accounted for in computing β.

If the receiver contains filters, the effect of the filters on the assumed white Gaussian noise present at the receiver input is computed. Based on a non-saturating receiver with an integrate-and-dump detector, the decrease in noise energy due to the filters is determined by evaluating and integrating the energy spectral response of the composite receiver filters. The input noise energy is thereafter decreased by this factor.

A.5.2   ADAPTIVE EQUALIZATION/PHASE TRACKING

The adaptive equalizer is modelled as a transversal filter with tap weights controlled by the LMS algorithm, as described in detail in Appendix C of reference 1. Decision-directed control of the weights is accomplished using the equalizer output samples, s. Input parameters for the equalizer are:

NTAP – the number of complex tap weights in the equalizer

ISP – the tap spacing given as the number of signal samples per tap

SK – the LMS algorithm constant of convergence

In operation, the program initializes the tap weights to produce an impulse response so that in the beginning the equalizer output is identical to its input. The transversal filter is modelled so that the successive tap weights multiply the input filtered signal samples spaced by ISP samples. These NTAP inputs are multiplied by the NTAP weights to form the instantaneous output quantity S. The LMS error quantity E is formed by subtracting the output S from D, the decision estimated for that output sample.

For each output S, corresponding to the correct sampling time, the error generated iterates the tap weights by the LMS algorithm. Following this update of weights, the input X is shifted one sample forward through the transversal filter to generate the subsequent output S. The weights are therefore updated only once per bit (in the I and Q channels) at the sampling time obtained by the bit sync loop. This process is continued until all NSMP samples of X have been shifted through the filter. This is accomplished by treating the input array X as a circular array due to its periodicity. The output array S is then used for obtaining the next estimate of bit sync.

The decision-directed quantity $D(v)$ is obtained from a quantizing performed on the complex output sample $S = I + jQ$ at the correct sampling instant. To review the LMS algorithm, the weights W are incremented by

$$\Delta W = SK \cdot E \cdot X*$$

where $S = W \cdot X$ is the output quantity, $E = D - S$ is the error, and SK is a small constant determining the rate of convergence. All quantities are complex except SK.

To track duobinary, $D(v)$ should be the three-level quantizing function for duobinary, defined as

$$
D(v) = \begin{cases}
1 - v; & .5 < v \\
-v; & -.5 < v < .5 \\
-1 - v; & v < -.5
\end{cases}
$$

A-28

The real part of D is based on quantizing the real part of S while the imaginary part of D is based on quantizing the imaginary part of S at the correct sampling times. For SQPSK duobinary, the in-phase term of $D(v)$ is computed at the inphase sampling instant while the quadrature term of $D(v)$ is obtained one-half of a bit duration (T_b) later at the quadrature sampling instant.

Since the adaptive equalizer under LMS control minimizes the mean square error, it also performs phase tracking. If no channel equalization is required, phase tracking can be accomplished by setting NTAP = 1 and using the same algorithm for error control based on the quantized sampled output decisions. This one-tap phase tracking algorithm is further discussed in Section 3.1. Note that the phase tracking algorithm also provides gain normalization for AGC action.

A.5.3   CLOCK TRACKING/DETECTION

The instant for sampling the waveform is determined in an iterative fashion which converges to the optimal value. Using the array S of equalizer output values, the integrate-and-dump detector uses the previously determined sync value ICL to obtain in-phase bit decisions every NSB samples. Quadrature bit samples for SQPSK are obtained starting at sample location ICL + NSB/2, obtaining outputs once every NSB samples from this initial location. These bit samples are stored in array T. In addition, an array R is formed by obtaining samples of the in-phase component of S at points midway $(T_b/2)$ between those selected for storage in T.

The samples in T, when bit sync is correct, occur at transitions for duobinary.* The samples in R occur midway between the transitions in the in-phase channel. Clock tracking is performed using only the in-phase samples. For QPSK, the quadrature tracking position is also at ICL while for SQPSK the quadrature tracking is located one-half bit duration away from that for the in-phase data.

The current clock tracking position can be advanced or retarded one sample for each iteration** through the equalizer, detector, and sampling loop. The sign (SGN) of each in-phase bit decision in array T is multiplied by the sample value displaced ahead by one-half of the bit duration T_b to obtain a value P_i. The P_i are summed over all LSEQ bit decisions and the sign of this sum is used to change the bit tracking location by one sample; i.e., ICL is either advanced or retarded by one sample value each iteration based on the polarity of the sum of the P_i.

*For conventional QPSK, the sampling is performed midway between bit transitions.

**Iteration is at the repetition rate of the periodic data sequence.

This updated value of ICL is used in the next iteration for equalization/phase tracking, detection, and clock tracking. Following convergence, of the bit tracking loop, the tracking position ICL will alternate between two adjacent locations on successive iterations through the loop. The integrate-and-dump detector then uses the final value of ICL obtained to form an array of detected bits.

A.5.4   VITERBI ALGORITHM

The Viterbi algorithm uses the detector outputs to perform a maximum likelihood demodulation of the duobinary data. A full description of the algorithm is found in Section 2.3.

The Viterbi algorithm correction procedure treats the inphase and quadrature soft bit decision samples as parallel independent bit streams so that, in effect, two parallel Viterbi algorithms are in operation and four states are stored at any instant of time. A table of precomputed filtered Gaussian noise samples is called and added to each bit decision sample to perform a Monte Carlo analysis of error rates. The error rate is measured by counting the actual errors made by the Viterbi algorithm when noise is present at the specified E_b/N_o. Output data taken from the path memory is delayed by 32 bits (the computer word length) and differentially decoded. The resulting data bits are then compared to the corresponding data bits actually transmitted to determine when an error is made.

In addition to the actual error count performed at the E_b/N_o used in the simulation, the error rate is obtained for a wide range of E_b/N_o using the estimation technique given in Appendix C.

APPENDIX B
SOFTWARE DESCRIPTION OF SIMULATION PROGRAM SIMB

This appendix covers software considerations of the computer program SIMB. The technical description of the operation and capabilities of SIMB are given in Appendix A. The following contains a description of all important system parameters, all input parameters, and all common statements in the program. In addition, descriptive writeups of the various subprograms called by SIMB are included.

An overall flow diagram of the main program is given in Figure B-1. Note that program SIMB is written in the FORTRAN IV language except for a small number of subprograms written in assembly language for efficiency, and the entire program has been developed on an IBM 370/145 computer system. The program is suited for either batch or timeshare operation.

B.1 INPUT PARAMETERS OF PROGRAM SIMB

To provide flexibility of application, program SIMB provides for a multiplicity of input parameters. These inputs permit structuring of the program flow to simulate a variety of system configurations and facilitate entry of the desired system and element parameters. All inputs are performed via NAMELIST statements so that any combination of parameters may be changed from default values in a given run without the necessity of entering those parameters whose values are not to be changed.

Three namelist statements exist. Namelist INPT controls the main program flow and contains all system parameters except the individual filter parameters and the receiver parameters. Namelist FLTR is called at each filter location to permit the user to enter the filter parameters used there. Namelist RCVR is called at the receiver to permit entry or changes of the receiver parameters and modes.
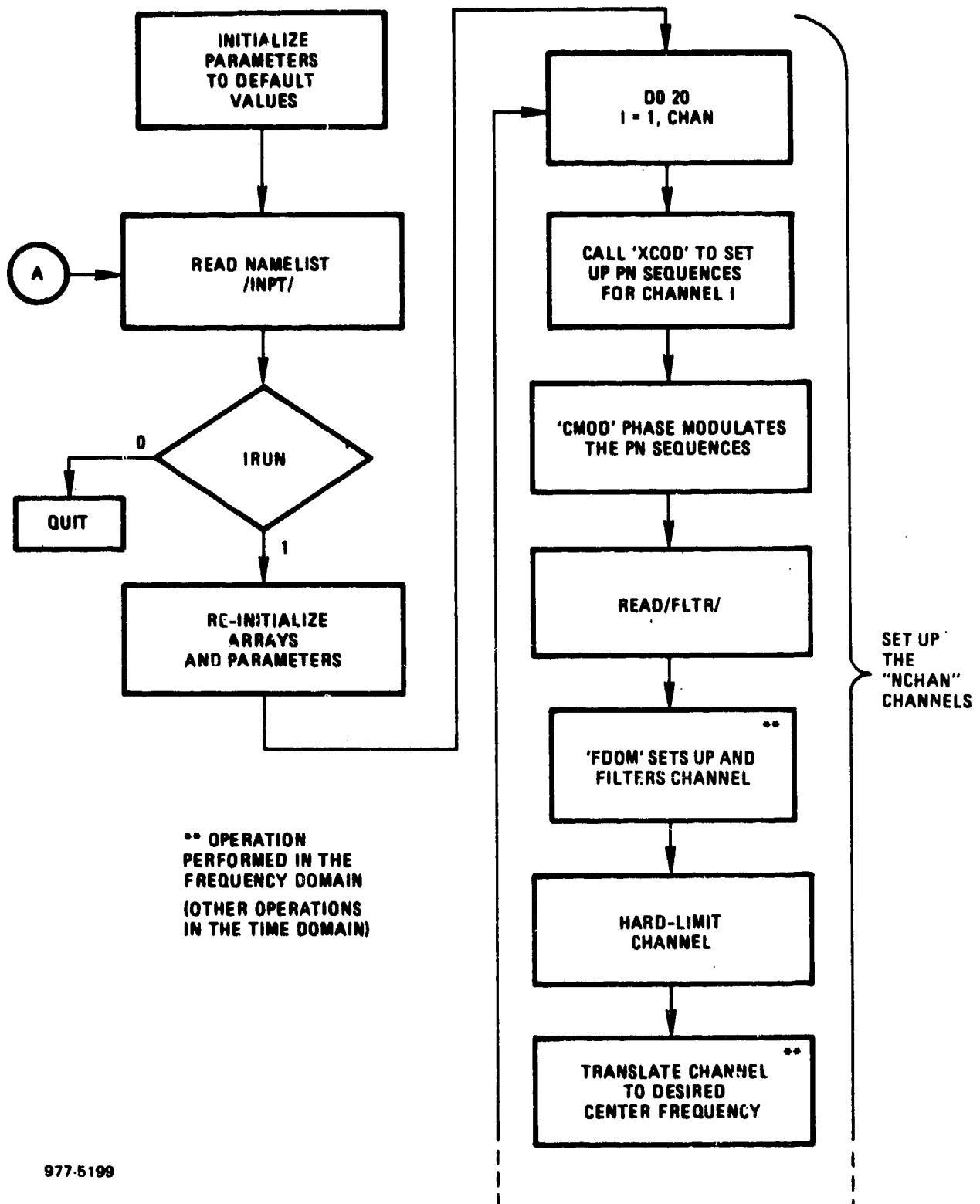
Figure B-1. Flow Diagram of Program

977-5199

SET UP
THE
"NCHAN"
CHANNELS

```
              ┌──────────────────┐
              │  ADD NEW CHANNEL │
              │  TO EXISTING     │
              │  CHANNELS        │
              └──────────────────┘

              ┌──────────────────┐
              │        20        │
              └──────────────────┘

        0    ◇ MDIST ◇   1, 2, 3
                              ┌──────────────────┐
                              │ 'DIST' ADDS    **│
                              │ CHANNEL PHASE    │
                              │ DISTORTION       │
                              └──────────────────┘

        0    ◇ LOCB ◇    1
                              ┌──────────────────┐
                              │   READ/FLTR/     │
                              └──────────────────┘

                              ┌──────────────────┐
                              │ 'FDOM' SETS UP **│
                              │ AND              │
                              │ FILTERS CHANNEL  │
                              └──────────────────┘

        0    ◇ MAMP ◇    1
                              ┌──────────────────┐
                              │ CALL 'AMP' TO    │
                              │ PERFORM          │
                              │ AMPLIFICATION    │
                              └──────────────────┘
```

977-5200

B-3

677-3752

READ/FLTR/

FDOM SETS UP **
AND FILTERS
SIGNAL

DO 40
I = 1,16

MEQUAL

1

2

0

ADAPTIVE
EQUALIZATION

ROTATE SIGNAL
BY PHASE $\dot{\varphi}_S$

ONE-TAP PHASE
TRACKER

BIT SYNC
ESTIMATION

40

INTEGRATE-AND-
DUMP DETECTOR

677-3763

```
                    │
                    ▼
            ┌───────────────────┐
            │      DO 60         │
   ┌────────▶     I = 1, MAX     │
   │        └───────────────────┘
   │                │
   │                ▼
   │        ┌───────────────────┐        ┌───────────────────┐
   │        │   ADD DETECTED    │        │     FILTERED      │
   │        │     BITS AND      │◀───────│      NOISE        │
   │        │   NOISE SAMPLES   │        │     SAMPLES       │
   │        └───────────────────┘        │ (COMPUTED OFFLINE)│
   │                │                     └───────────────────┘
   │                ▼
   │        ┌───────────────────┐
   │        │     VITERBI       │
   │        │    ALGORITHM      │
   │        └───────────────────┘
   │                │
   │                ▼
   │        ┌───────────────────┐
   │        │   COUNT ERRORS/   │
   │        │  UPDATE MEAN AND  │
   │        │VARIANCE OF DECISIONS│
   │        └───────────────────┘
   │                │
   │                ▼
   │        ┌───────────────────┐
   └────────│       60          │
            └───────────────────┘
                    │
                    ▼
            ┌───────────────────┐
            │   PERFORM BIT     │
            │  ERROR ESTIMATION │
            └───────────────────┘
                    │
                    ▼
            ┌───────────────────┐
            │   GO TO   Ⓐ       │
            └───────────────────┘
```

677-3863

This section lists the input parameters of each namelist together with the default value of the parameter. The default value is that value used by the program in lieu of a different value specified by the user. Inputs are entered via the appropriate namelist statement. Any number of the possible parameters may be changed on any input call. The last value given to a parameter is used for subsequent runs until changed by user specification oi a new value. The format for entering data via the namelist INPT call is

b & INPT b P1 = xx, P2 = xx, P8 = xx, P5 = xx, & END

where b designates a space, & is the ampersand character, P represents a parameter name, and xx represents the numerical value assigned to that parameter. Value types must match the variable type (integer, real, complex, etc.). The parameters to be changed may be input in any sequence. The corresponding namelists FLTR and RCVR are handled with the same format. Following the last run, the input

b & INPT b IRUN = 0, & END

terminates execution of the program.

PARAMETER NAME	DESCRIPTION	TYPE*	UNITS	DEFAULT VALUE
Accessing Signal Specification				
MPSK	(=2) biphase; (=4) quadriphase	I	----	4
NSMP	Number of sampling points	I	----	1024
LSEQ	Length of PN sequences used	I	----	54
QDEL	Displacement of quadrature data from in-phase data	R	Bits	0
ISQ	(=0) quadriphase; (=1) staggered quadriphase	I	----	0
NCHAN	Number of channels through transmitter	I	----	1
CPR	Array specifying power of each channel (CPR (1) is center signal power)	R	dB	0
Channel Filter Locations				
LOCA	Sets up channels, filters and frequency offsets each as desired (=0) no set up; (=1) set up the NCHAN channels	I	----	1
LOCB	Indicates channel filter preceding nonlinear amplifier; (=0) no filter; (=1) filter	I	----	0
LOCC	Indicates channel filter following non-linear amplifier; (=0) no filter; (=1) filter	I	----	0
LOCD	Indicates filter in receiver (=0) no filter ; (=1) filter	I	----	0
System Nonlinearities				
LIM	Transmitter hard limiter; (=0) on; (=1) off	I	----	0
MAMP	(=0) no amplifier; (=1) amplifier	I	----	0
TYPE	(=0) linear amplification; (=1) TWT; (=2) soft limiter; (=3) hard limiter; (=4) amplitude characteristic of a Phase III TWT (=5) amplitude characteristic of Phase II TWT	I	----	0
BO	TWT backoff (absolute value)	R	dB	3
GAIN	Amplifier gain (optional entry)	R	dB	3

*I = Integer, R = Real.

PARAMETER NAME	DESCRIPTION	TYPE*	UNITS	DEFAULT VALUE
PHASE	(=0) no phase shift; (=1) Berman-Mahle; (=2) linear phase; (=3) truncated linear phase; (=4) AM-PM characteristic of a Phase III TWT; (=5) AM-PM characteristic of Phase II TWT	I	----	0
PHS	Phase shift (for PHASE = 2 or 3)	R	Degrees/dB	0
MDIST	(=0) no phase distortion; (=1) sin phase; (=2) cos phase; (=3) parabolic phase	I	----	0
SK	Peak phase error (see text)	R	Degrees	5
FR	Normalized ripple frequency (see text)	R	----	1
MAGC	Indicates mode of automatic gain control (=0) normal automatic operation (=1) uses value AGCC, AGC defeated	I	----	0
AGCC	Value of AGC used when MAGC = 1	R	----	1
MSYN	Indicates mode of bit sync loop (=0) normal automatic operation; (=1) uses value XDEL, sync loop defeated	I	----	0
XDEL	Value of sync delay used when MSYN = 1	R	----	0
MEQUAL	Indicates IF equalizer in receiver (=0) no equalizer; (=1) adaptive equalizer; (=2) one tap phase tracker	I	----	2
NTAP	Number of equalizer taps	I	----	16
MREF	Mode of obtaining desired response (=0) training sequence; (=1) decision feedback	I	----	0
ISP	Tap spacing in number of signal samples per tap	I	----	8
ISHIFT	Relative displacement between input signal samples and desired response samples (in number of samples)	I	----	0

The parameters are grouped in the left margin as: Channel Phase Distortion (PHASE, PHS, MDIST, SK, FR), AGC (MAGC, AGCC), Bit Sync (MSYN, XDEL), Adaptive Equalizer (MEQUAL, NTAP, MREF, ISP, ISHIFT).

*I = Integer, R = Rate.

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PARAMETER NAME	DESCRIPTION	TYPE*	UNITS	DEFAULT VALUE
EBN	Value of receiver input signal-to-noise ratio	R	dB	16
IDISP	Mode determining spectral plotting (=0) no plots; (=1) plot data	I	---	0
IRUN	Run execution indicator (=0) terminate execution; (=1) run next case	I	---	1

*I = Integer, R = Rate.

B.3   INPUT PARAMETERS FOR NAMELIST FLTR

PARAMETER NAME	DESCRIPTION	TYPE*	UNITS	DEFAULT VALUE
MFILT	Type of filter used (=0) no filter; (=1) Butterworth; (=2) Chebyshev; (=3) Gaussian; (=5) phase distortionless maximally-flat filter response	I	---	0
BT	One-sided filter bandwidth (normalized to bit rate)	R	---	1
NP	Number of filter poles $(1 \leq NP \leq 15)$	I	---	5
RIP	Chebyshev filter ripple amplitude	R	dB	.05
FCENT	Filter center frequency offset (normalized to bit rate)	R	freq. offset/ bit rate	0

*I = Integer, R = Rate.

B.4   INPUT PARAMETERS FOR NAMELIST RCVR

PARAMETER NAME	DESCRIPTION	TYPE*	UNITS	DEFAULT VALUE
MFILT	Type of filter used (=0) no filter; (=1) Butterworth; (=2) Chebyshev; (=3) Gaussian; (=5) phase-distortionless maximally-flat characteristic	I	---	5
BT	One-sided filter bandwidth (normalized to bit rate)	R	---	.333
NP	Number of filter poles ($1 \leq NP \leq 15$)	I	---	5
RIP	Chebyshev filter ripple amplitude	R	dB	.05
SK	Adaptive equalizer convergence constant	R	---	.001
EBN	Receiver input E_b/N_o	R	dB	16
MCL	Bit sync tracking loop mode (=0) tracking loop on; (=1) loop off, track at delay ICL	I	---	0
ICL	Fixed loop tracking position (for MCL = 1)	I	---	0
IRUN	Run execution indicator (=0) return to main program; (=1) rerun data through receiver	I	---	0

*I = Integer, R = Rate.

B.5 <u>PARAMETERS IN COMMON STATEMENTS USED IN SIMA</u>

B.6 <u>COMMON/PAMP/PHASE, TYPE, GAIN, BO, PHS, VO, GI</u>

PHASE = phase characteristic of nonlinear amplifier

TYPE = amplitude characteristic of nonlinear amplifier

GAIN = gain slope of amplifier

BO = TWT backoff value in decibels

PHS = number of degrees per dB value for amplifier phase characteristic

VO = internally computed TWT output voltage at given backoff

GI = internally computed scaling of amplifier input to produce the desired backoff.

B.7 <u>COMMON/FLT/FNC, PP(15, 2), WC, NP, MFILT, RIP</u>

FNC* = normalization factor for filters to produce unity amplitude response at filter center frequency

PP*(15, 2) = poles and residues of filter

WC = 3 dB filter bandwidth, in radians

NP = number of filter poles

MFILT = type of filter (Butterworth, Chebyshev, or Gaussian)

RIP = Chebyshev filter ripple amplitude, in decibels.

B.8 <u>COMMON/SIG/TBD, MDIST, P(4), G(4), SK, FR, LSEQ</u>

TBD = bit duration (nominally = 1)

MDIST = type of phase distortion in channel

P(4) = four values of modulator phase (degrees)

G(4) = four values of modulator gain (decibels)

SK = peak channel phase error (degrees)

FR = normalized channel phase error frequency (see text)

LSEQ = number of chips in PN sequence.

B.9 <u>COMMON/PLL/V(3), WW(3), E(3)</u>

V(3) = Array for phase tracking loop storing frequency values

W(3) = array storing internally computed loop coefficients

E *(3) = array storing output error voltages for loop.

---

*Implies parameter is complex.

B.10 COMMON/DEM/T, W, NSMP, NSB, NTAP, EBN, ICL, ISP, LSEQ, IDEL, ID1, ID2

$T(128)$ = array of soft bit decisions based on optimal sampling time. In-phase and quadrature bit decisions alternate.

$W(64)$ = array of complex adaptive equalizer weights.

NSMP = number of samples in signal array Z.

NSB = number of samples per bit in signal array Z.

NTAP = number of weighted taps in adaptive equalizer.

EBN = receiver input E_b/N_o, in decibels.

ICL = clock bit tracking location for I channel.

ISP = equalizer tap spacing in number of signal samples per tap.

LSEQ = length of PN sequences used.

IDEL = displacement of Q data bit transitions from I data bit transitions.

ID1, ID2 = optimal (I and Q) bit delays through the channel, as determined by correlating the channel input and output data bits.

B.11 COMMON/NOIS/AN

$AN*(64,64)$ = array of complex filtered noise samples with zero mean and unity variance. These samples represent the (unscaled) noise components at the detector output.

B.12 COMMON/MID/RI, RQ

$RI(64)$ = array of the LSEQ pseudonoise bits used to modulate the I channel.

$RQ(64)$ = array of the LSEQ pseudonoise bits used to modulate the Q channel.

B.13 COMMON/VAL/BITS, EX1, EX2, DA, IA, IC

BITS = incoming soft bit decision to Viterbi algorithm.

$EX1(64, 2)$ = array of the running sum of the LSEQ metric differences output by the Viterbi algorithm.

$EX2(64, 2)$ = array of the running sum of the LSEQ squared metric differences output by the Viterbi algorithm.

$DA(2)$ = temporary storage of the current (I and Q) metric differences (AM).

$IA(2)$ = temporary storage of the current path memory I0 (for I and Q).

$IC(2)$ = temporary storage of the current path memory I1 (for I and Q).

B.14   COMMON/DAT/Z, NSMP, IDELB, ANSB, J1

Z(1024) – complex array of signal samples

NSMP – number of samples in array Z

IDELB – number of samples delay of data in quadrature channel from data
in in-phase channel (for QPSK)

ANSB – number of samples per bit in array Z

J1 – optimum bit sync offset (in samples)

B.15   COMMON/FFT/M, INV, S

M(3), INV(256), S(256) explained in IBM writeup of Fast Fourier
Transform HARM

B.16   DESCRIPTION OF SUBPROGRAMS CALLED BY SIMB

This section contains subroutine and function descriptions to enable under-
standing of their purpose and usage. Pertinent parameters are described and sub-
programs called are listed. Remarks are given when required concerning considerations
or limitations involved when using the routine. The technical description of the functions
performed in these subroutines is given in Appendix A.

SUBROUTINE: ALGV

PURPOSE

Based on signal + noise samples, ALGV calls the Viterbi algorithm, computes the mean and variance of the difference, performs differential decoding of the detected bits, and determines whether an error (incorrect decision) was made.

USAGE

Call ALGV (NM, PE, JJ, I). Calling program must contain the statements COMMON/DEM/-, COMMON/VAL/-, COMMON/MID/-.

DESCRIPTION OF PARAMETERS

NM - counter including the effect of the decoding delay.

PE - contains the total number of bit decision errors that occur.

JJ - parameter determining whether bit is from the I or the Q channel.

I - parameter denoting which of the LSEQ bits is being detected.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

VITAL.

SUBROUTINE: AMP

PURPOSE

AMP simulates several nonlinear amplifiers, including both amplitude and phase effects on the time-sampled input signal, by calls to function NLN. AMP can model hard and soft limiters, Travelling Wave Tube (TWT) amplifiers, as well as simulating only the phase or only the amplitude characteristics of such amplifiers.

USAGE

Call AMP(X, NSMP). Calling program must include the following statements COMMON/PAMP/-,EXTERNAL OPPT.

DESCRIPTION OF PARAMETERS

TYPE – type of nonlinear amplifier amplitude characteristic to be modelled; (=0) linear amplification; (=1) Berman-Mahle TWT model; (=2) soft limiter; (=3) hard limiter; (=4) amplitude characteristic of a Hughes' TWT; (=5) amplitude characteristic of the Phase II TWT.

PHASE – form of nonlinear amplifier phase shift characteristic to be modelled; (=0) no phase shift; (=1) Berman-Mahle phase characteristic; (=2) linear phase shift, in degrees per dB; (=3) truncated linear phase shift; (=4) AM-PM characteristic of a Hughes' TWT; (=5) AM-PM characteristic of Phase II TWT.

PHS – phase shift in degrees per dB (for TYPE = 2).

GAIN – gain slope of amplifier.

BO – backoff of TWT from maximum output power (dB).

VO – internally computed output voltage at the specified backoff.

GI – internally computed scaling of input signal to produce the desired backoff.

REMARKS

Subroutine AMP accepts the NSMP time samples $\underline{X}$ of the input signal and scales the amplitude and phase of each sample to simulate the action of the nonlinear amplifier being modelled. AMP returns the array $\underline{X}$ of output samples to the calling program.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

NLN, AGC, ADB, OPPT, NRR, FMIN.

SUBROUTINE: CERR

PURPOSE

CERR accepts an array of detector output quantities (for both the I and Q channels) and determines the resulting probability of error and system degradation at the user specified signal-to-noise ratios.

USAGE

Call CERR (LSEQ, PWRN, SNR1, SNR2, DSNR). Calling program must contain the following statements COMMON/DCD/-.

DESCRIPTION OF PARAMETERS

LSEQ - number of bits in the input PN sequence.

SNR1 - first signal-to-noise ratio at which probability of bit error is computed (in dB).

SNR2 - last signal-to-noise ratio at which probability of bit error is computed (in dB).

DSNR - step size between SNR, in dB.

PWRN - precomputed change in input noise energy due to noise passage through receiver filters and/or equalizer.

REMARKS

CERR accepts detected bits through the COMMON array SUM. If no noise filtering is performed, PWRN should be initialized to unity.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

AWERC, ERR.

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FUNCTION: CMOD

PURPOSE

CMOD is used to phase modulate an input time sample X. CMOD can model an ideal biphase or quadriphase modulator or simulate a phase modulator with amplitude and phase errors.

USAGE

Y = CMOD(X, J). Calling program must contain the following statements COMMON/FLT/-;COMMON/SIG/-;COMPLEX CMOD, Y.

DESCRIPTION OF PARAMETERS

X - input (real) time sample to be phase modulated.

J - channel in which sample X is to be placed; (=0) I channel; (=2) Q channel.

P - array of four phase locations (nominally 0°, 90°, 180°, 270°).

G - array of four amplitude values (nominally 0 dB). (Note that P and G can be externally changed to other values.)

SUBROUTINE: CORE

PURPOSE

CORE correlates received bits with transmitted bits to determine correct bit alignment for Viterbi algorithm.

USAGE

Call CORE (LSEQ). Calling program must contain the statements COMMON/MID/-, COMMON/DEM/-.

DESCRIPTION OF PARAMETERS

LSEQ - length of PN sequences used.

REMARKS

CORE correlates the detected bits with the transmitted bits independently for the I and Q channels. The alignment positions found are returned through COMMON/DEM/ as parameters IDI and IDQ.

SUBROUTINE: CORNS

PURPOSE

CORNS develops correlated noise samples, assuming white Gaussian received noise samples, to account for the presence of receiver filters and/or equalization in the receiver.

USAGE

Call CORNS (K, AN, BN, IR, DD). Calling program must contain the following statements: COMMON/FFT/-   and COMMON/DAT/-

DESCRIPTION OF PARAMETERS

K - normally = 0, set = 1 at the beginning of a new set of LSEQ input samples.

AN - in-phase noise sample returned to calling program.

BN - quadrature noise sample returned to calling program.

IR - parameter controlling Gaussian generating program SNORM. Initialize IR = 9 at first call to CORNS.

DD - array containing frequency response of receiver, including filter and equalizer response.

REMARKS

If K = 0, CORNS sets up NSMP correlated noise samples based on the composite receiver frequency response stored in complex array DD. Thereafter, each call returns a successive noise sample based on the integrate-and-dump output.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

SNORM, HARM.

SUBROUTINE: DEMOD

PURPOSE

Subroutine DEMOD uses an array of filtered noise samples to perform an error estimation analysis of the Viterbi algorithm based on the detected samples. DEMOD computes the differentially decoded error rate over a range of receiver input E_b/N_o values.

USAGE

Call DEMOD(Z). Calling program must contain the following statements: COMMON/MID/-, COMMON/FFT/-, COMMON/FLT/-, COMMON/NOIS/-, COMMON/DEM/-, COMMON/VAL/-, COMPLEX Z(1024).

DESCRIPTION OF PARAMETERS

Z - complex array of time samples at receiver input

T - array of bits from the integrate-and-dump detector output

AN - array of filtered noise samples

REMARKS

DEMOD displays the estimated probabilities of bit errors over the range of input E_b/N_o = 5 dB to 17 dB and the actual error count at the user specified E_b/N_o.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

ALGV, AWERFC.

SUBROUTINE: DISPLA

PURPOSE

DISPLA accepts an array of NSMP frequency samples and generates all calls for a CALCOMP plotter.

USAGE

Call DISPLA (Z, IPL).

DESCRIPTION OF PARAMETERS

Z – array of NSMP complex frequency samples to be plotted.

IPL – parameter initializing plotter. IPL = 0 on first call to DISPLA in program; IPL = 1 thereafter.

SUBROUTINES AND PROGRAM FUNCTIONS REQUIRED

Normal calls to CALCOMP plotting subroutines.

FUNCTION: DIST

PURPOSE

DIST models several forms of phase distortion in a communications channel, specifically sinusoidal, cosinusoidal and parabolic phase variation with frequency and step changes in phase at specified frequencies. The function returns the phase associated with the frequency (s) specified.

USAGE

Y = LIST(S). Calling program must contain the following statements COMPLEX DIST, Y, S; COMMON/FLT/-; COMMON/SIG/-.

DESCRIPTION OF PARAMETERS

S - complex input frequency (radians/sec).

MDIST - type of phase distortion modelled; (=0) no distortion; (=1) sinusoidal phase variation with frequency; (=2) cosinusoidal phase variation with frequency; (=3) parabolic phase variation with frequency.

FR - normalizes ripple frequency (see text).

SK - peak phase error for MDIST = 1 or 2 phase error at frequency FR for MDIST = 3.

SUBROUTINE: EQOUT

PURPOSE

EQOUT simulates a transversal filter and multiplies an incoming

sampled time waveform by the weights to obtain an output sample.

USAGE

Call EQOUT (Y, S, I). Require COMMON/DEM/-.

DESCRIPTION OF PARAMETERS

Y - array of input time samples

S - output time sample

I - index of the sample of Y falling at the first tap of transversal filter

W - array of tap weights

NTAP - number of tap weights

ISP - spacing between tap weights

SUBROUTINE: ERREST

PURPOSE

ERREST uses the array of detected bits to estimate the bit error rate at the specified receiver input E_b/N_o.

USAGE

Call ERREST (PWRN, EBN). Calling program must contain the statements: COMMON/DEM/-.

DESCRIPTION OF PARAMETERS

PWRN - resulting noise power after receiver filtering and equalization

EBN - receiver input E_b/N_o for which error rate is to be determined

REMAKRS

ERREST uses the Viterbi estimation discussed in Appendix C of this report.

SUBROUTINE: IAND

PURPOSE

To perform logical ANDs of two integer arguments, bit-by-bit. IAND is in IBM assembly language.

USAGE

IPROD = IAND (I1, I2).

DESCRIPTION OF PARAMETERS

I1 - (INTEGER *4) - First operand. It is returned unchanged.

I2 - (INTEGER *4) - Second operand. It is returned unchanged.

IAND - (INTEGER *4) - The bit-by-bit logical product (AND) of the first and second argument is returned as the function value.

REMARKS

FORTRAN integer variables are represented in binary, two's-complement notation on the IBM 370 system.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

None.

SUBROUTINE: IXOR

PURPOSE

To perform exclusive ORs of two integer arguments, bit-by-bit. IXOR is in IBM assembly language.

USAGE

ISUM = IXOR (I1, I2).

DESCRIPTION OF PARAMETERS

I1 - (INTEGER *4) - First operand. It is returned unchanged.

I2 - (INTEGER *4) - Second operand. It is returned unchanged.

IXOR - (INTEGER *4) - The bit-by-bit modulo-two sum (exclusive OR) of the first and second argument is returned as the function value.

REMARKS

FORTRAN integer variables are represented in binary, two's-complement notation on the IBM 370 system.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

None.

SUBROUTINE: RECFIL

PURPOSE

RECFIL is called at the location of each receiver filter to determine the reduction of noise energy produced by that filter. White Gaussian channel noise is assumed present at the receiver input.

USAGE

Call RECFIL (CN, MFILT, DDD).

DESCRIPTION OF PARAMETERS

CN -- ratio of noise energy at filter output to that present at filter input.

MFILT -- receiver filter type.

DDD -- array containing frequency response of filter.

SUBROUTINE: MSRG

PURPOSE

To simulate a modular shift-register binary code generator of any length
to 32 bits. MSRG is in IBM assembly language.

USAGE

IOUT = MSRG(ITAP, ISTATE).

DESCRIPTION OF PARAMETERS

ITAP - (INTEGER *4) - Feedback tap code in reversed notation. The
        least -significant-bit of ITAP is the coefficient (0, 1) of the
        next-to-highest degree term of the polynomial. Coefficients of
        lesser degree terms are then placed in successively higher order
        bits of ITAP. Consequently, generators with less than 32 stages
        are specified by filling the unused most-significant-bit positions
        with zeros. The coefficient of the highest degree term is omitted.

ISTATE - (INTEGER *4) - Present state (i.e., contents) of the shift-
        register. The direction of shifting is from the most-significant-
        bit to the least-significant-bit. The new state is returned in
        ISTATE.

MSRG - (INTEGER *4) - The output of the shift register is returned as
        the integer value (0, 1) MSRG.
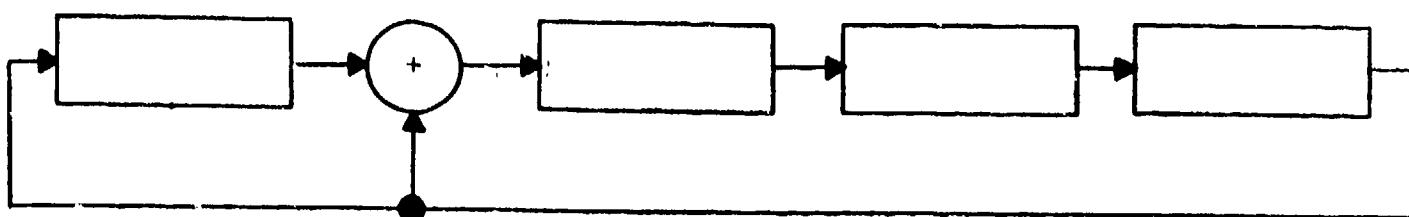
SUBROUTINE: SETRCV

PURPOSE

Contains receiver functions of filtering, phase tracking, bit sync, and adaptive equalization. SETRCV also contains the integrate-and-dump detector.

USAGE

Call SETRCV (Z, LOCD, NCHAN). Calling program must contain the following statements: COMMON/DEM/-, COMMON/FFT/-, COMMON/FLT/-, COMMON/NOIS/-. The following namelist is read from SETRCV: NAMELIST/ RCVR/-.

DESCRIPTION OF PARAMETERS

Z   - complex array of time samples into receiver.

LOCD   - determines presence of receive filter.

NCHAN   - number of accessing signals.

T   - array of bits from the detector output.

REMARKS

SETRCV performs a Monte Carlo equalization and tracking on the filtered signal plus noise samples at a user specified E_b/N_o. This is defaulted to 16 dB if not user specified via namelist RCVR. Array Z is returned to the calling program unchanged; i.e., without additive noise. Output array T contains the output bits from the integrate-and-dump detector in the order of an I sample followed by a Q sample.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

FDOM, FBUT, HARM, EQOUT, SNORM.

SUBROUTINE: SMPLS

PURPOSE

SMPLS is used for obtaining correct bit synchronization.

USAGE

Call SMPLS (R, Z). Calling program must contain the statement:

COMMON/DEM/-.

DESCRIPTION OF PARAMETERS

Z - array of input signal samples

R - array of in-phase output samples at one-half bit displacement from those in T

T - array of in-phase and quadrature output samples, based on the current sampling estimate

REMARKS

Arrays R and T contain the appropriate signal samples for use in the bit tracking loop.

SUBROUTINE: SNORM

PURPOSE

To generate independent normally distributed samples. SNORM is in IBM assembly language.

USAGE

V = SNORM (IR).

DESCRIPTION OF PARAMETERS

IR – (INTEGER *4) – For the first entry, IR must contain a positive integer of the form 4n = 1, n is an integer. Thereafter, IR will contain an integer generated by the subprogram for use on the next entry to the subprogram.

SNORM – (REAL *4) – The resultant normally distributed random number with zero mean and unit variance.

REMARKS

The method of generating the samples is algorithm FL_5 described in J. H. Ahrens and U. Dieter, "Extensions to Forsythe's Method for Random Sampling from the Normal Distribution", to appear.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

None.

SUBROUTINE: VITAL

PURPOSE

This subroutine contains the Viterbi algorithm for maximal-likelihood decoding of the duobinary data.

USAGE

Call VITAL (V, AM, IO, I1, IS, D).

DESCRIPTION OF PARAMETERS

V - soft decision input bit

IO, I1 - path memories

AM - metric difference state

IS - present differentially decoded bit state (0 or 1)

D - absolute value of current metric difference

REMARKS

The operations performed in subroutine VITAL are described in Section 2 of this report.

SUBROUTINE: XCOD

PURPOSE

Generation of PN sequences for biphase and quadriphase channels.

USAGE

Call XCOD, (RI, RQ, ISEQ, KSGQ, MVIT, LSEQ, ISTAT, JS, IJS, ITAP). Calling program must contain the following statements COMMON/DCD/-; EXTERNAL VITERB; DIMENSION RI(64), RQ(64), ISEQ(32), KSEQ(32).

DESCRIPTION OF PARAMETERS

ISEQ - PN bit sequence for in-phase data.

KSEQ - PN bit sequence for quadrature data.

RI - encoded bit sequence for in-phase channel.

RQ - encoded bit sequence for quadrature channel.

LSEQ - number of bits in PN sequence.

ISTAT - current state of PN sequence generator.

JS - number of bits in maximal length PN sequence.

IJS - parameter controlling flow of XCOD.

REMARKS

Subroutine XCOD is called to set up independent PN bit sequences for the I and Q channels of each signal to be transmitted.

SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED

MSRG, IAND, IXOR.

ADDITIONAL SUBPROGRAMS USED

The following functions and subroutines are used to perform specific functional calculations and will be described in a briefer fashion than the preceding subprograms.

A.   FUNCTION: DB

PURPOSE

DB accepts a real quantity R and returns the value of R in decibels

$$S = 10 \log_{10} R$$

CALLING THE SUBPROGRAM

$S = DB(R)$.

B.   FUNCTION: ADB

PURPOSE

ADB accepts a quantity S expressed in decibels and returns the value of S as a real number

$$R = 10^{S/10}$$

CALLING THE SUBPROGRAM

$R = ADB(S)$.

C.   FUNCTION: WERFC

PURPOSE

WERFC accepts a quantity R and returns the Weber error function evaluated at R

$$S = \frac{1}{\sqrt{2\pi}} \int_{R}^{\infty} e^{-x^2/2} dx$$

CALLING THE SUBPROGRAM

$S = WERFC(R)$.

D.   FUNCTION: AWERFC

PURPOSE

AWERFC accepts a value of the Weber error function S and returns the argument R of the error function.

CALLING THE SUBPROGRAM

R = AWERFC(S).

E.   FUNCTION: AGC

PURPOSE

AGC accepts the array Z containing N complex numbers and returns the rms value of these numbers.

CALLING THE SUBPROGRAM

Y = AGC(Z, N).

F.   FUNCTION: FMIN

PURPOSE

Function FMIN finds the argument X of an external function F which minimizes an external function F by performing a Golden Search over the interval [X1, X2]. Parameter EPS determines the accuracy required in locating the exact minimum.

CALLING THE SUBPROGRAM

X = FMIN(F, X1, X2, EPS); EXTERNAL F.

G.   COMPLEX FUNCTION: FFR

PURPOSE

FFR uses the poles computed for a filter to determine the complex filter response at a frequency S.

CALLING THE SUBPROGRAM

R = FFR(S); COMMON/FLT/-.

H.   COMPLEX FUNCTION: FDOM

PURPOSE

FDOM accepts the complex array Z containing N frequency response samples and multiplies them by N values of an external function F evaluated at the same frequencies as the corresponding samples of Z. FDOM returns the array Z of multiplied samples.

CALLING THE SUBPROGRAM

Y = FDOM(F, Z, N); COMMON/SIG/.

I.   SUBROUTINE: ERR

PURPOSE

ERR accepts an array SUM of L detector output values, computes the probability of error PER of each value at a given signal-to-noise ratio (not in decibels), and averages these L probabilities to return the average probability of error PER.

CALLING THE SUBPROGRAM
CALL ERR(PER, SUM, X, L).

J.   SUBROUTINE: FBUT

PURPOSE

FBUT sets up the frequency response of a phase distortionless filter having a 5-pole maximally-flat amplitude response. FBUT is called from FDOM if MFILT = 5.

For single carrier operation, namelist/FLTR/ is called once at point LOCA. For multiple carriers, namelist/FLTR/ is called NCHAN times at location LOCA to permit required filtering and frequency offset for each carrier. The last call to /FLTR/ at LOCA is the baseband carrier on which detection is performed. Thus, this last call to /FLTR/ should have FCENT = 0.

One precaution must be considered for multiple carrier operation besides the multiple calls to /FLTR/ at location LOCA. The bit sync loop can yield erroneous sync due to the multiplicity of signal crossings. To avoid these problems the following procedure can be used when running such cases:

a.   First, run the system with all elements present and only a single carrier. Determine the value of SYNC obtained as output.

b.   Next, run the multiple carriers through the system but defeat the bit sync loop by entering MSYN = 1. Also enter the value of SYNC previously obtained by means of input parameter XDEL. This parameter is input through the namelist/INPT/ call.

Finally, a plot of the spectral response of the system at locations LOCA, LOCB, LOCC, and LOCD can be obtained by specifying the locations desired and entering IDISP = 1.

USING PROGRAM SIMB

Program SIMB has been constructed to facilitate user interaction in setting up the system to be simulated and for entering the specific program parameters desired. Multiple passes may be made through the program on each run of SIMB. As previously mentioned, namelist inputs are used throughout the program for data input. Only those parameters which are different from default values (or different from the previous pass) need be entered at each namelist call.

Each namelist statement (/INPT/, /FLTR/, or /RCVR/) is prompted when required. Namelist /INPT/ is called to begin each new run and /RCVR/ is called upon entry to the receiver portion of the program. Namelist /FLTR/ is called, for single carrier operation, at those filter locations (LOCA, LOCB, LOCC, and LOCD) specified through the namelist /INPT/. Note that for LOCD, /FLTR/ is called following /RCVR/.

APPENDIX C
ESTIMATING PROBABILITY OF ERROR OF VITERBI ALGORITHM

This appendix describes a technique to estimate the probability of error P_e of a soft decisions (i.e., unquantized) demodulator incorporating the Viterbi algorithm for a channel with intersymbol interference and/or convolutional coding. The goal is to estimate P_e when the number of bits is too small to measure P_e by directly counting errors made by the algorithm. (For example, to measure $P_e = 10^{-4}$ requires counting errors in at least 10^5 bits; otherwise, the statistical fluctuations prevent an accurate result from being obtained.)

The technique depends on identifying the error mechanism in the Viterbi algorithm. Let us review the algorithm briefly. A metric and associated path memory of decisions for prior metric comparisons is stored for each state. When the soft decisions for the symbols of a node are received, the storage for each state is updated on the basis of a comparison between the metrics for the possible paths leading to the state. With a binary algorithm, there are two paths, and a binary comparison is made to discard the poorer path. The other path is retained and is called the survivor. Considering only the comparison for the correct state at each node, an error is necessarily made by the algorithm when the correct path is not the survivor. This happens if the metric difference has the wrong polarity.

Because of the additive noise, the metric difference at each comparison is a random variable. By collecting appropriate statistics on the distribution of this random variable, the probability of error can be estimated from a small sample size even though errors are not actually made by the algorithm, and this is the basis for the technique to be described.

C.1   THE IDEAL MEMORYLESS BINARY CHANNEL

To begin, let us study convolutional coding on the ideal memoryless binary channel with Gaussian noise, for which each node is statistically identical. If the metric comparison at a node is made between the correct word and the most likely incorrect word (which has Hamming distance d_{free}), the metric difference will be a sum over

the soft decisions for d_{free} symbol differences; hence, is Gaussian distributed. The mean m of the distribution is set by the bit amplitude, while the variance σ^2 is proportional to the noise power. Hence, the probability of incorrect decision for this comparison is determined by the ratio m/σ, which is proportional to $\sqrt{E_b/N_o}$.

The metric difference does not have a Gaussian distribution exactly because of the effect of prior comparisons to select surviving words, but we can proceed on the approximate basis of fitting a Gaussian distribution to the sample mean $\hat{m}$ and sample standard deviation $\hat{\sigma}$, measured over a number of bits. This enables an estimate of the probability of making an incorrect decision for any metric comparison. Multiplying by the expected number of bit errors n_{bit} resulting from an incorrect decision provides the desired estimate of the probability of bit error P_e for the Viterbi algorithm. Thus, denoting the Gaussian distribution by $\Phi(x)$, we approximate the probability of error P_e as a function of E_b/N_o by

$$ P_e \cong n_{bit} \left\{ 1 - \Phi\left(\frac{\sqrt{E_b/N_o}}{\sqrt{(E_b/N_o)_{actual}}} \ \hat{m}/\hat{\sigma} \right) \right\} \tag{.1} $$

where $\hat{m}$ and $\hat{\sigma}$ are measured at $(E_b/N_o)_{actual}$. It is better to measure $\hat{m}$ and $\hat{\sigma}$ at each E_b/N_o for which P_e is to be estimated, but this increases computation time to obtain a curve of P_e as a function of E_b/N_o.

If the metric difference at each successive node is an independent random variable, we can compute roughly the number of bits n needed to obtain a desired accuracy. The rms fluctuation in the ratio $\hat{\sigma}/\hat{m}$ is approximately $1/\sqrt{2n}$ relative to the true value[9]. Specifying this fluctuation to be 0.1 dB, or 2.3 percent, requires n = 922. Thus, the measurement should extend over several thousand bits for good statistical convergence.

There still is uncertainty as to what value to assign to the expected number of bit errors n_{bit}. When the erroneous metric comparison selects an incorrect word, the number of bit errors is one or more, depending on the particular incorrect word. Simulations[10;p. 135] for a rate-1/2 code of constraint length 7 show that the expected number of bit errors in an error burst is approximately 4. (This is also a good estimate if the data is differentially decoded after error correction.)

Figure C-1 plots the estimate of P_e for a rate-1/2 code as a function of E_b/N_o from (1) by averaging over 10,000 bits, setting $n_{bit} = 4$. Comparison is made to the upper bound for Viterbi decoding[10;p. 144]. The estimate taken at $(E_b/N_o)_{actual}$ 4 dB appears to be quite accurate over the range of interest of low error rates. Note that no errors were actually made by the Viterbi decoder. As a check, two additional runs were made with a different starting point for the random number generator. The spread of results is marked in Figure C-1 by the vertical bar at $E_b/N_o = 5$ dB. The uncertainty in required E_b/N_o to achieve a specified error rate is seen to be 0.3 dB. As a further comparison, an error count was made over 100,000 bits at $E_b/N_o = 3$ dB. A total of 71 errors was made, which is statistically reliable. The measured error rate is plotted in Figure C-1, and is close to the theoretical upper bound. Hence, the estimate of P_e is somewhat optimistic at this high error rate.

These results for the ideal PSK channel give confidence in the estimation technique, at least for low error rates where an actual error count is impractical. For the number of bits selected for averaging, the lowest $(E_b/N_o)_{actual}$ should be used for which there are no decoding errors, indicating the correct path is a survivor in the Viterbi algorithm after the comparison at each successive node.

C.2   THE CHANNEL WITH INTERSYMBOL INTERFERENCE

If the channel has intersymbol interference, such as due to a narrow filter bandwidth, P_e can be estimated by a modification of the averaging procedure. Simulations of this case assume a periodic data sequence, so that the metric differences would be periodic also except for the fluctuations due to noise. Then, the sample mean and standard deviation in the metric difference are measured separately for each bit in the period L, averaging over the repetitions. Denoting the measurements as $\hat{m}_i$ and $\hat{\sigma}_i$ for $i = 1$ to L, the approximate probability of error becomes

$$ P_e = \frac{n_{bit}}{L} \sum_{i=1}^{L} \left\{ 1 - \Phi \left(\frac{\sqrt{E_b/N_o}}{\sqrt{(E_b/N_o)_{actual}}} \hat{m}_i/\hat{\sigma}_i \right) \right\} \qquad (2) $$

where $\hat{m}_i$ and $\hat{\sigma}_i$ are measured at $(E_b/N_o)_{actual}$.

Note that the predominant contribution to P_e is from the metric comparisons where $\hat{m}_i/\hat{\sigma}_i$ is lowest.
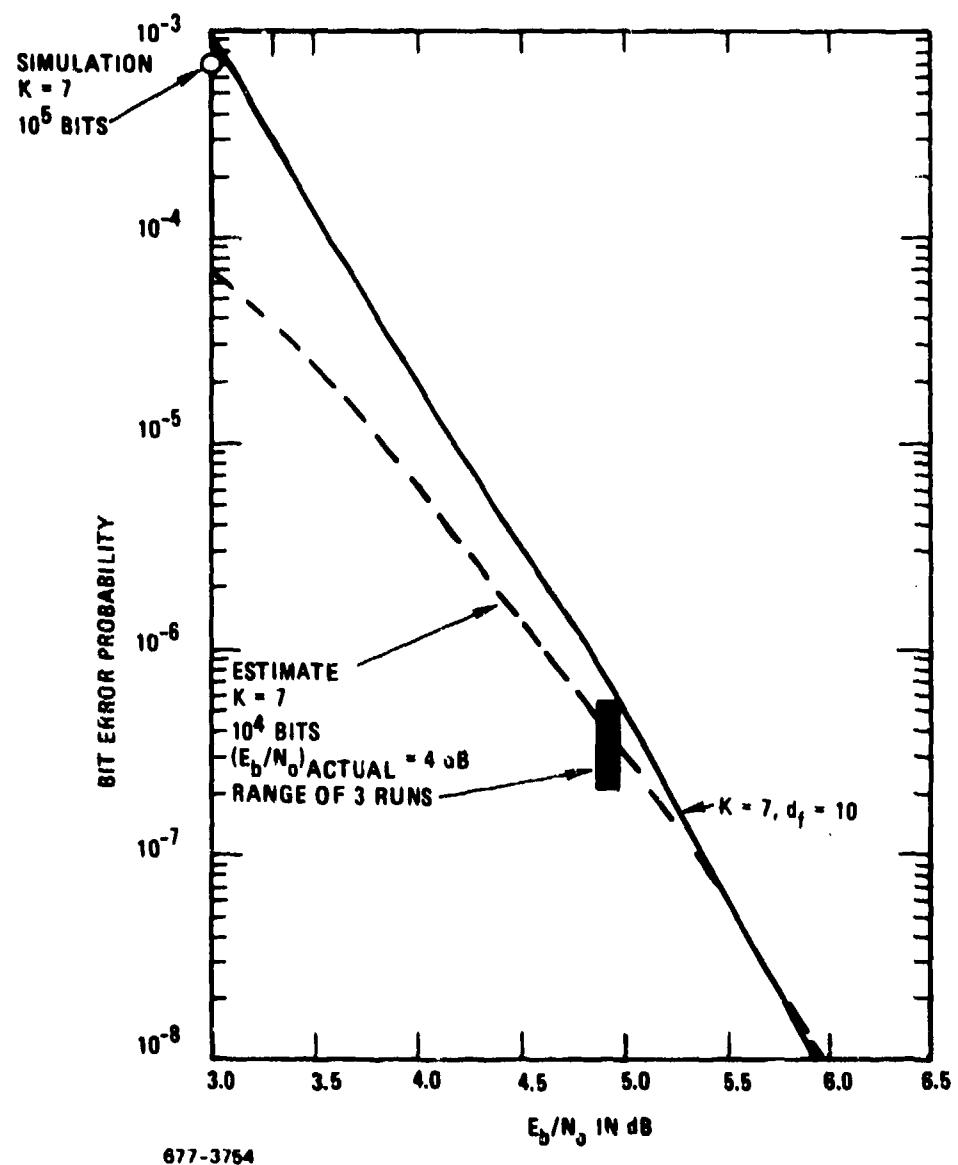
Figure C-1. Comparison of Performance Estimate With Theoretical Upper Bound and Actual Error Counts

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C.3   RATE-3/4 CODING ON MEMORYLESS BINARY CHANNEL

Equation (2) also has application to the memoryless binary channel when the code is periodically varied. An example of this is a rate-3/4 code derived from a rate-1/2 code by deleting symbols. The deletion pattern is different for successive data bits but repeats after 4 symbols have been generated from 3 data bits. Thus, (2) is used here with $L = 3$.

Figure C-2 plots estimates of P_e for a rate-3/4 code derived from a rate-1/2 code of constraint length 7. The estimates are obtained by averaging over 9000 data bits.

Also plotted in Figure C-2 are actual error counts. One set of runs took the decoder output from the path memory of the state with maximum metric, using a path memory length of 28, which is adequate for a rate-1/2 code.[13] However, a by-product of the estimation technique is that the decoder is supplied with knowledge of the correct state; hence, the decoder output can be taken from the path memory of the correct state. This is equivalent to having an extremely long path memory in the decoder. Figure C-2 indicates approximately 1 dB improvement in performance at $P_e = 10^{-4}$ when the path memory is much longer than 28 bits.

Comparison between the estimated and the actual performance shows the estimation technique is optimistic for the rate-3/4 code on the memoryless binary channel. For a decoder with a long path memory, the discrepancy is tolerable, being less than 1 dB.

C.4   PERFORMANCE ESTIMATION FOR DUOBINARY

As a first application of the estimation technique to a channel with inter-symbol interference, we consider SQPSK duobinary with Viterbi algorithm demodulation. The channel is adaptively equalized to the desired duobinary response with the tap weights of the equalizer controlled by the LMS algorithm from the error with respect to duobinary decisions on the individual bit samples (decision-directed control). The Viterbi algorithm significantly reduces the error rate, but in this simulation the data bits output from the algorithm are not utilized to improve the equalizer control.

The duobinary decision on a soft decision of amplitude v is defined as follows.
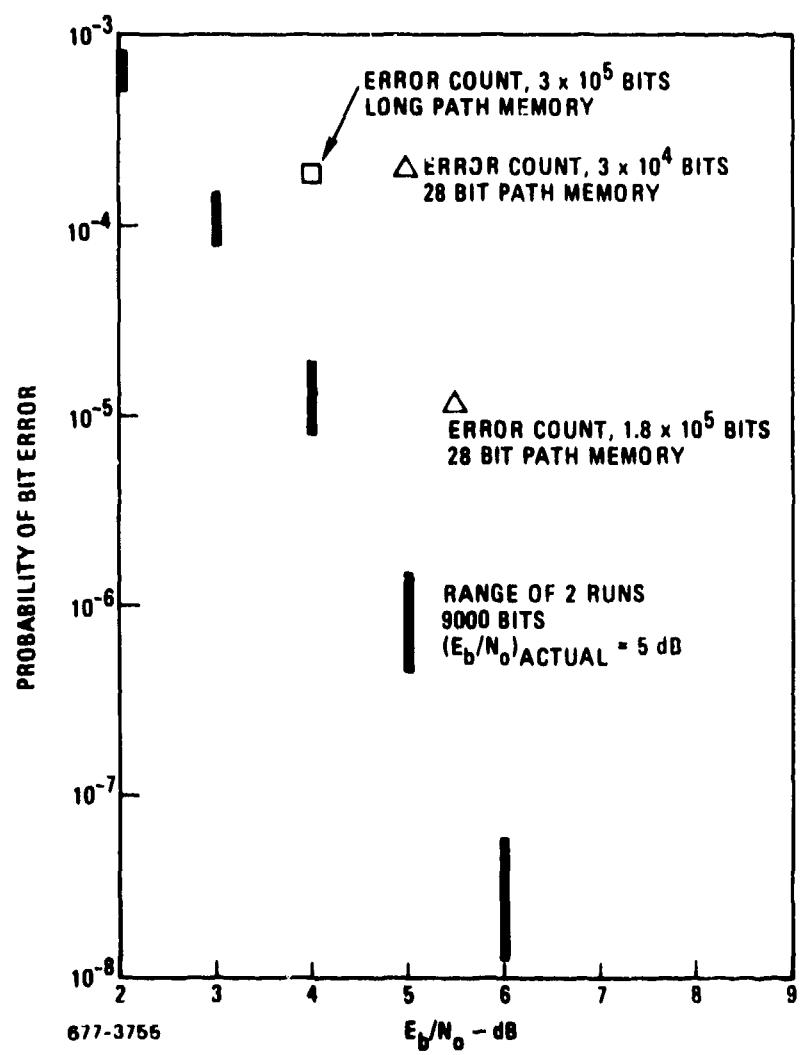
Figure C-2. Ideal Rate-3/4 Viterbi Decoding, Derived From $K = 7$ Rate-1/2 Code

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$$.5 < v \implies +1.0 \quad \text{hard decision}$$

$$-.5 \cdot v \cdots .5 \implies 0. \quad \text{hard decision} \qquad (3)$$

$$v < -.5 \implies -1.0 \quad \text{hard decision}$$

In the following simulations of duobinary, both the transmitter and the receiver have symmetrical 5-pole Butterworth filters.

Figure C-3 plots the estimated performance obtained from a simulation with a period of 64 random data bits (64 inphase and 64 quadrature transmitting at 3 bps/Hz). After equalization, 100 repetitions (total of 12,800 bits) are used to compute the estimation according to (2). The same equalizer tap weights were retained for three additional runs to estimate probability of error from 12,800 bits, each run having its own random sequence of bits and noise. The spread of the estimation is plotted in Figure C-3, along with some error rates based on actual error counts. The agreement is good between the estimation and the actual error counting, and the spread in the estimation from the four different runs gives an uncertainty of 0.3 dB in the E_b/N_o needed for 10^{-5} error rate.

C.5 PERFORMANCE EVALUATION FOR RATE-1/2 CODED DUOBINARY

As a second application of the estimation technique to a channel with intersymbol interference, consider the duobinary SQPSK channel with a rate-1/2 code. The channel is adaptively equalized to the desired duobinary response, with the tap weights of the equalizer controlled by the LMS algorithm with error derived from correct bits (training sequence). With a rate-1/2 code and a Viterbi decoder for duobinary, it has been found possible to transmit at the symbol rate of 4 bps/Hz, so that the data rate is 2 bps/Hz.

The simulation has a period of 64 data bits. Figure C-4 shows the estimate of P_e from a measurement over 100 repetitions (6400 bits) after convergence of the equalizer, or a constraint length K of both 5 and 7, setting $n_{bit} = 4$ in (2). Simulation results of error counting for K = 5 are also plotted and show excellent agreement with the estimate. Note that the error count at $E_b/N_o = 6$ dB is taken over 500 repetitions (32,000 bits).

It is interesting to observe that the rate-1/2 coded duobinary system displays a roughly constant coding gain relative to uncoded duobinary, over the range of interest. With a constraint length 7 code, the coding gain is 4.5 dB; furthermore, the data rate is 2/3 of that for uncoded because of the higher symbol rate transmitted.

The figure plots PROBABILITY OF BIT ERROR (vertical axis, from 10^{-5} to 10^{-0}) versus E_b/N_0 IN DECIBELS (horizontal axis, from -4 to 10).

Curve labels: DPSK, PSK, △PSK

ESTIMATE
(4 RUNS AT
$E_b/N_0 = 16$ dB)

ERROR COUNT

DUOBINARY SQPSK
8-TAP EQUALIZER
DATA RATE = 3 BPS/HZ
5-POLE BUTTERWORTH FILTERS

677-3786
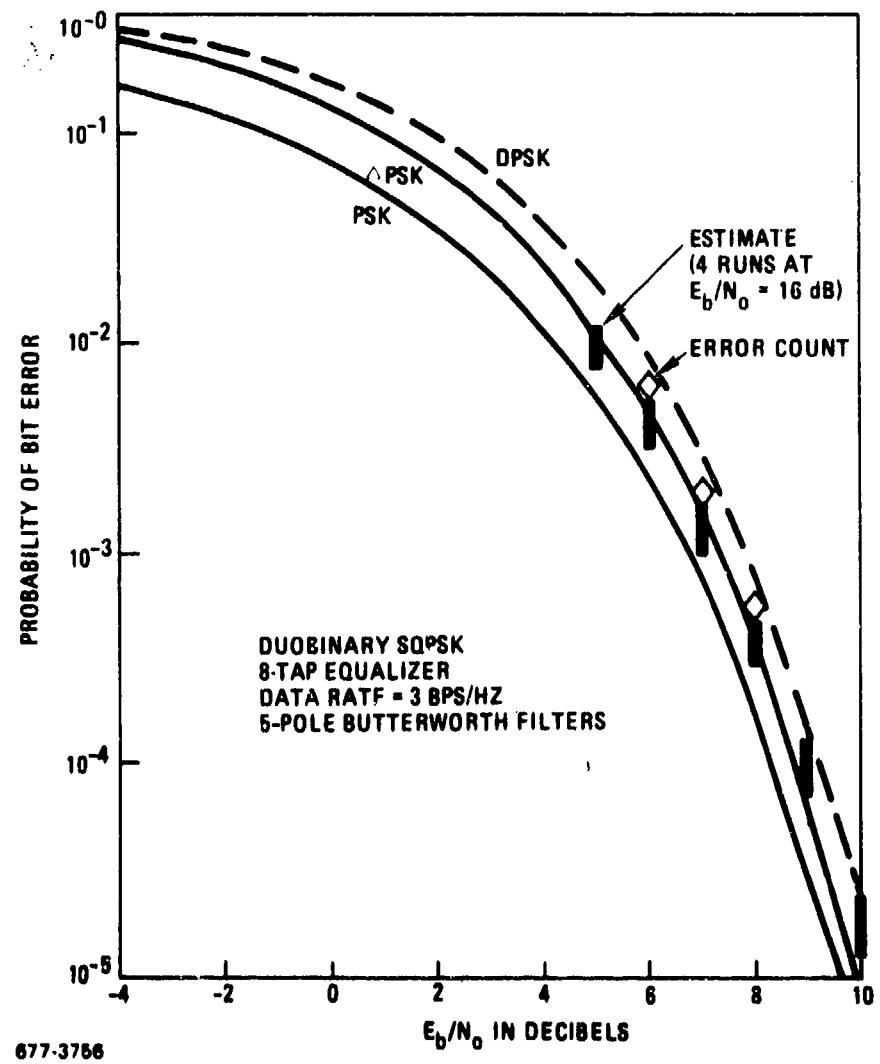
Figure C-3. Duobinary SQPSK Performance

5-POLE BUTTERWORTH FILTERS
8-TAP EQUALIZER
RATE-1/2 CODING
DATA RATE = 2 BPS/Hz
SYMBOL RATE = 4 BPS/Hz

DPSK

△PSK

PSK

ESTIMATE, 6400 BITS
$(E_b/N_o)_{ACTUAL}$ = 6 dB

K = 5

K = 7

ERROR COUNT
K = 5

PROBABILITY OF BIT ERROR

E_b/N_o IN DECIBELS

677-3757
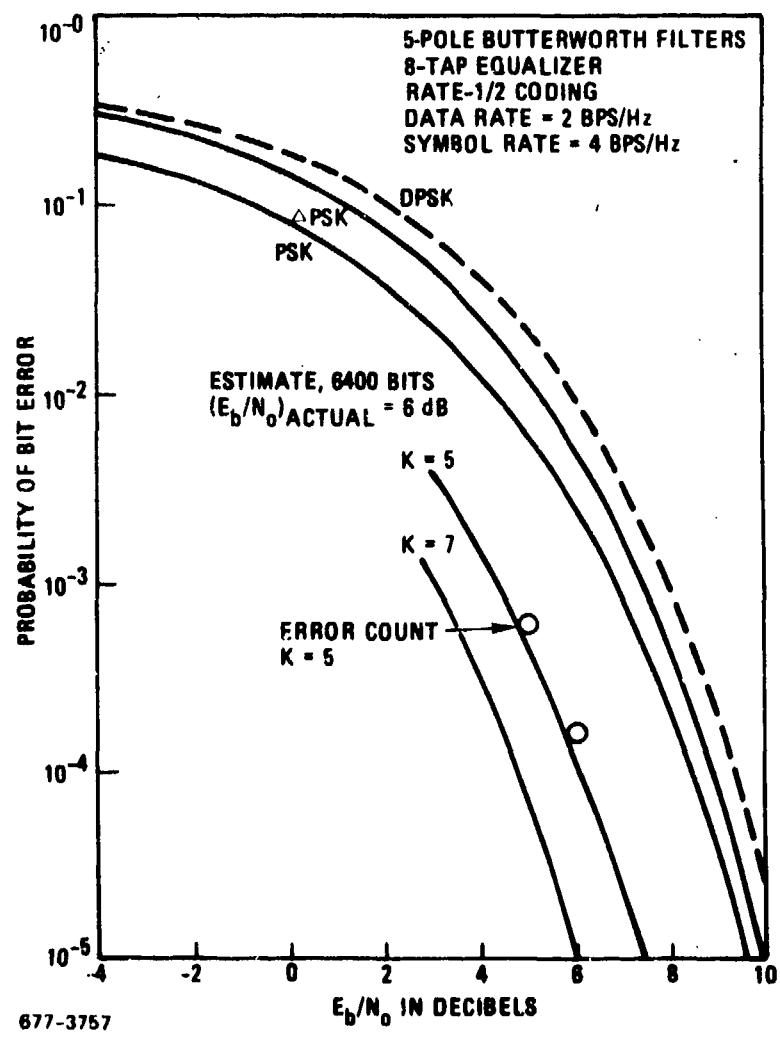
Figure C-4. Performance of Duobinary SQPSK With Rate-1/2 Coding

C-9

C.6   CONCLUSIONS

A technique to estimate probability of error for the Viterbi algorithm applied to decoding a convolutional code and/or a channel with intersymbol interference has been described. This method produces a reasonably accurate estimate from a small sample where an error count would not be statistically meaningful. The technique fits a Gaussian distribution to the sample mean and sample variance of the metric differences. The probability of error is given by the tail of the fitted distribution.

There is good agreement between the estimate and available performance results from bounds and from actual error counts based on large samples; hence, the estimation technique appears quite accurate at error rates of 10^{-5} and lower.

APPENDIX D
FEASIBILITY OF MODIFYING HARRIS MD-1002 MODEM
TO DUOBINARY SQPSK OPERATION

This appendix examines the functional implementation of the Harris MD-1002 modem with respect to the feasibility of modifying it from conventional SQPSK operation to duobinary SQPSK operation. The conceptual implementation approach has been described in Section 3.7; now, the specific assemblies (or cards) which must be modified or replaced in the MD-1002 are to be identified. Information is taken from the MD-1002 Technical Manual[11].

While an ideal objective for the modification would be to substitute new assemblies for existing ones on a plug-in card basis, there is the additional requirement that new interconnections usually must be made between the assemblies. Hence, the ideal objective is unattainable, although card replacement to enable either conventional or duobinary operation may be feasible after the new interconnections have been provided.

Modifications are to the receiver only. The duobinary SQPSK transmitter generates the same IF output as a conventional SQPSK transmitter. However, it is necessary to provide a linear-phase, maximally-flat, sharp cutoff filter in the transmitter IF output. An identical filter is also inserted in the receiver IF input. The filter 3-dB bandwidth (two-sided) should be in the range R/3 to 2R/3, where R is the total data rate in bps, as found in Section 3.5.

D.1   OVERALL MODIFICATION CONCEPT

Figure D-1, taken from reference 11, is a general block diagram of the unmodified RF Demodulator in the MD-1002 modem. The Receive Bit Synchronizer, not shown in Figure D-1, demodulates the I and Q bits and outputs a serial bit stream (interleaving I and Q differentially-decoded bits). In the unmodified modem, the Receive Bit Synchronizer is not involved in carrier phase tracking, which is done by a X4 multiplication process on the IF signal after narrow band filtering. The I and Q detector outputs from the RF Demodulator are accepted by the Receive Bit Synchronizer, which makes quantized soft decisions on the I and Q bits. However, only the sign bits have significance in the absence of error correction coding.
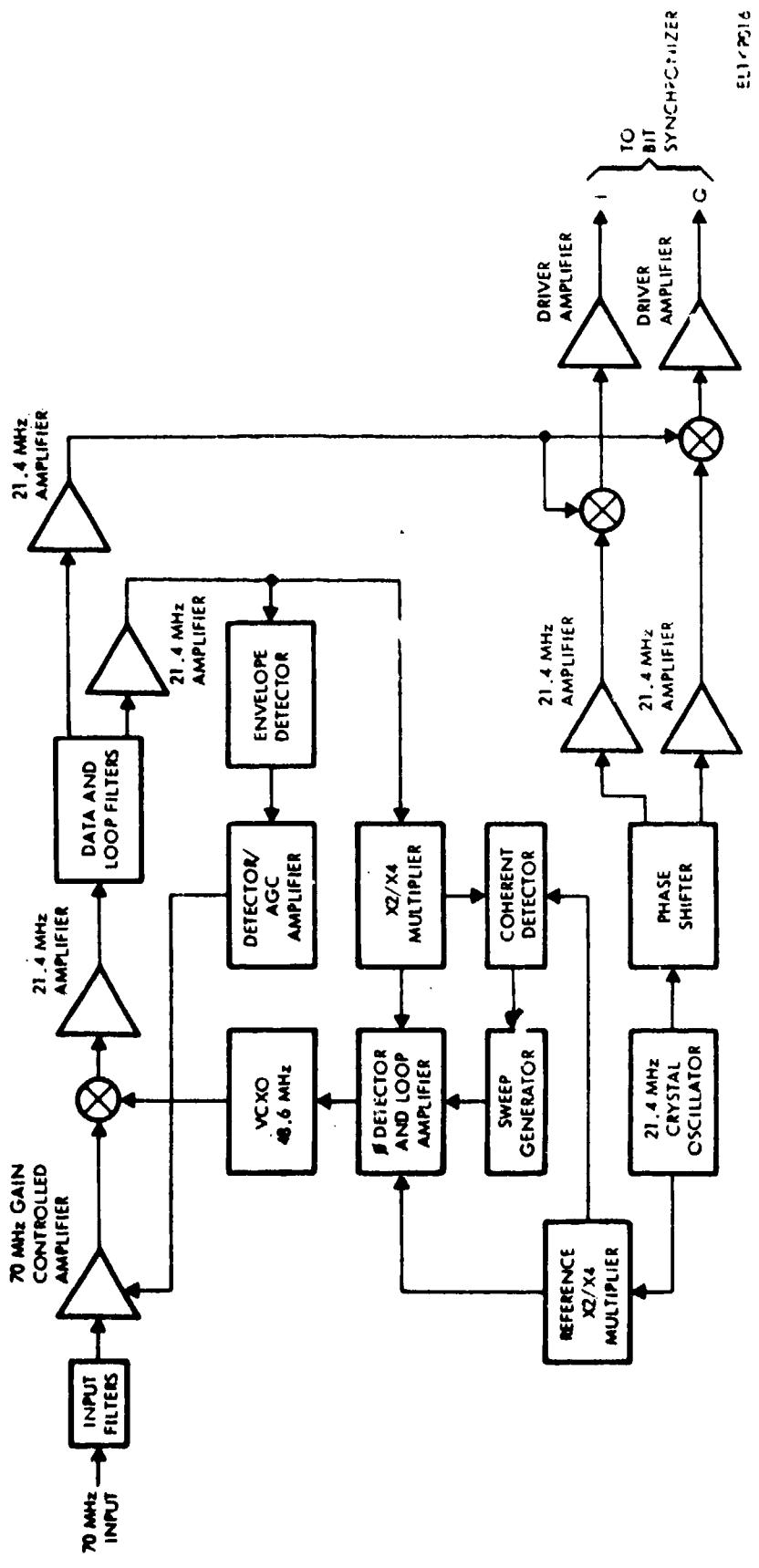
Figure D-1. General Block Diagram of RF Demodulator in MD-1002 Modem

Figure D-2 is a general block diagram of the receiver modified for duo-binary SQPSK. Now, the Receive Bit Synchronizer is shown explicitly because it is an integral part of the carrier phase tracking process. Also, soft decisions are utilized by the Duobinary Viterbi Algorithm. The I and Q samples are taken at twice the I-channel symbol rate (i.e., at the total bit rate). These samples are processed to develop an error voltage fed back to the 48.6 MHz VCXO for carrier phase tracking and for a synchronization indicator to stop the sweep. The "phase" samples taken from an integrator straddling the bit transitions are input to the Duobinary Viterbi Algorithm, which demodulates the data. The "data" samples from an integrator centered on the bits would be used for conventional binary decisions in the unmodified modem, but in the modified modem are involved only in the carrier tracking and bit synchronization functions.

D.2   MODIFICATIONS TO RF DEMODULATOR

Figure D-3 is a functional block diagram of the RF Demodulator, broken down into the constituent assemblies. The assemblies to be modified are now described.

PLL Ampl And Sweep Ckt (A2A24). The multiplier U3 is eliminated, and the DC input to the summer driving AR2 is taken from the decision-directed carrier tracking error produced by a new assembly described later. The loop filter for conventional BPSK has a 176 Hz bandwidth, and would be usable for duobinary SQPSK.

X2/X4 Mult (A2A20). This assembly need not be modified. However, the circuits from multiplier U1 to the left could be eliminated. Only the gain control signal output from AR1 to the AGC loop amplifier remains functional.

Quadrature Detector (A2A35). This assembly need not be modified, but is not functional except for the Reset to the sweep control logic. The output from AR1 is eliminated, being replaced by the DC output from a new assembly described later.

Reference X2/X4 Mult (A2A22). This assembly need not be modified. However, only the 21.4 MHz oscillator output is retained, and all circuits from AR1 to the left could be eliminated.

Thus, only one assembly (A2A24) in the RF Demodulator actually must be modified. The inputs P1-13 and P1-26 to A2A24 are eliminated, and a new DC input is taken from the decision-directed carrier tracking error produced by a new assembly.
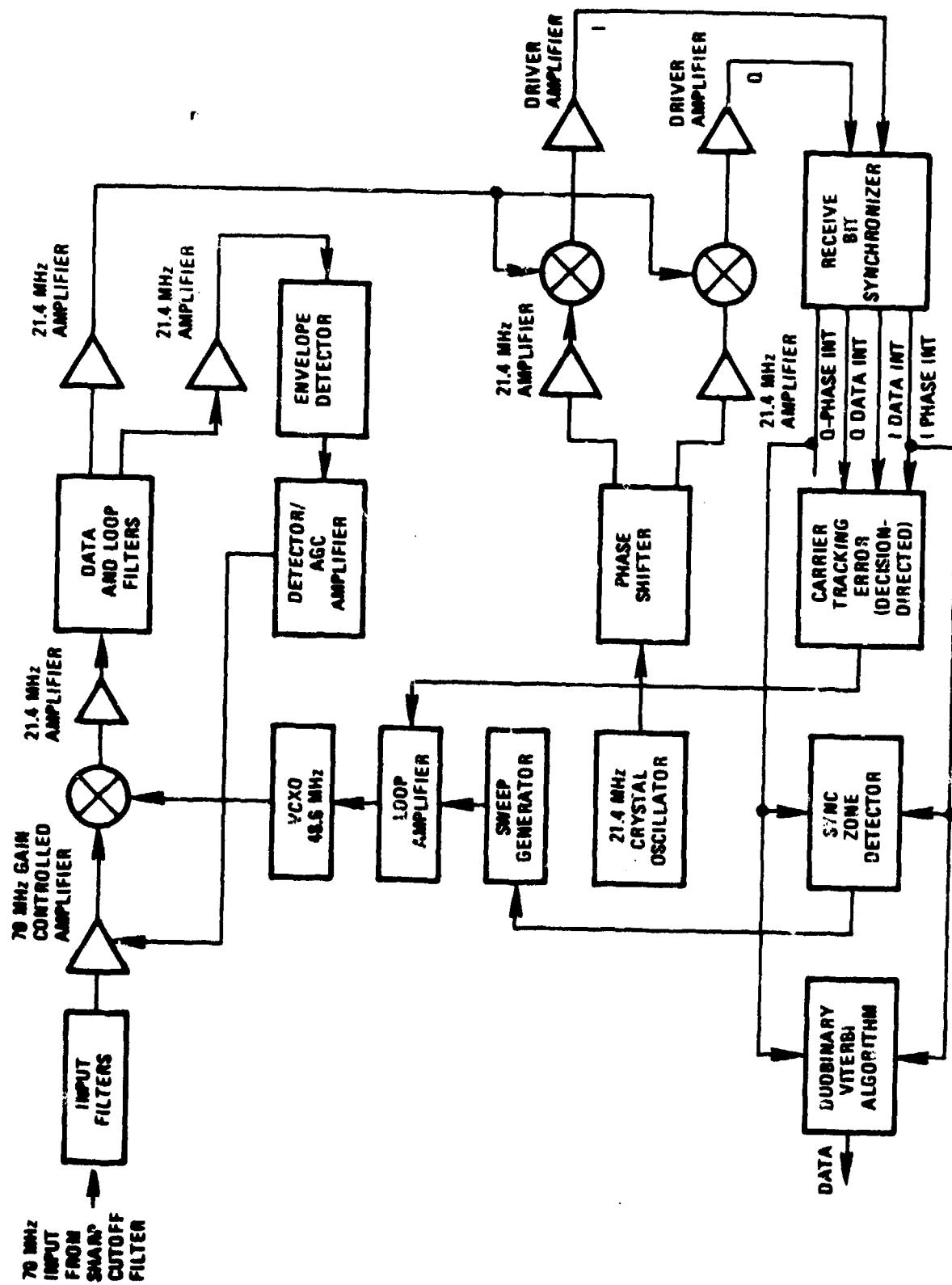
Figure D-2. General Block Diagram of Modem Modified for Duobinary

977-6201

677-3788
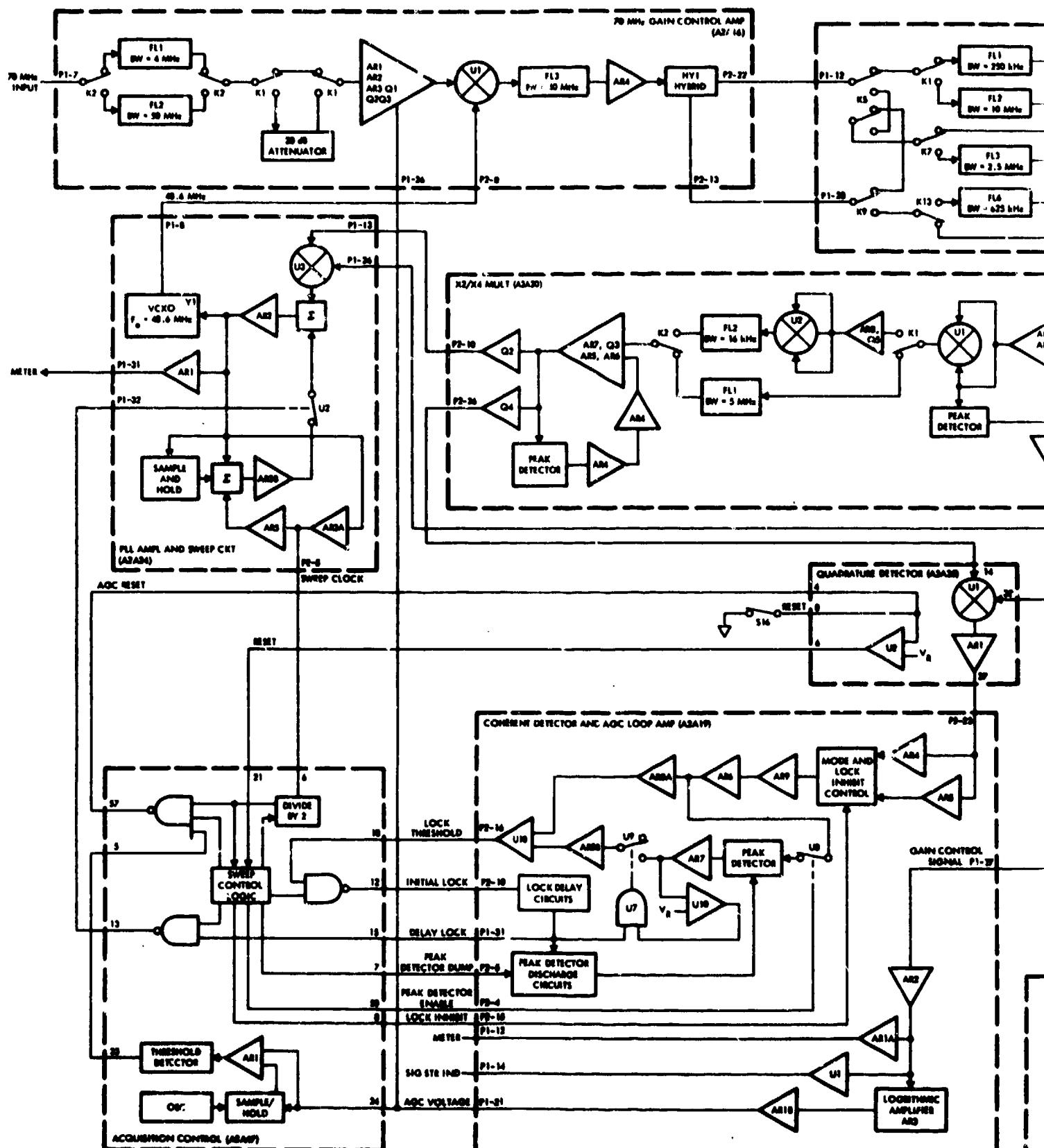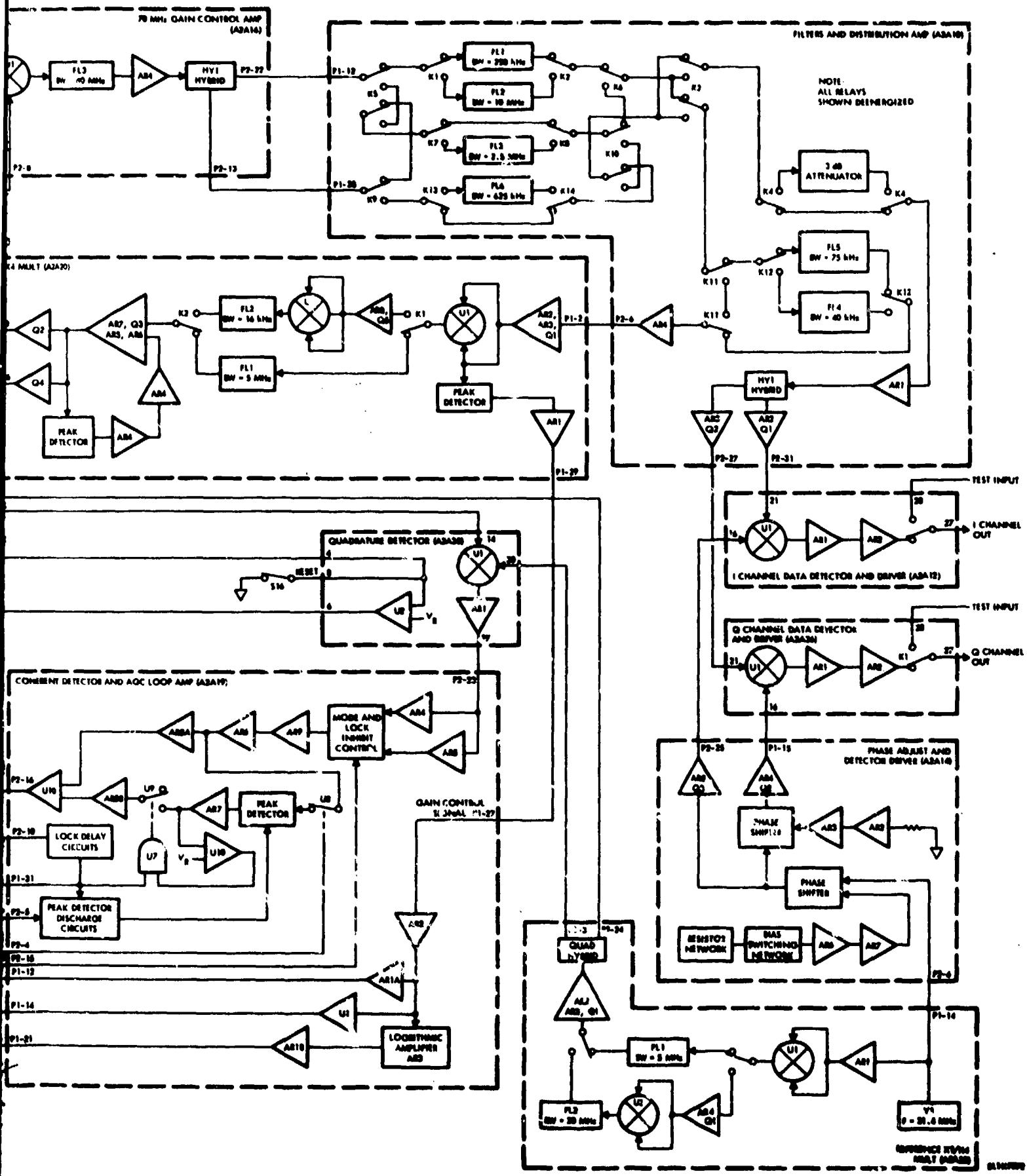
Figure D-3. Functional Block Diagram of RF Demodulator, FO-23

D-5

MODIFICATIONS TO RECEIVE BIT SYNCHRONIZER

Figure D-4 is a functional block diagram of the Receive Bit Synchronizer, broken down into the constituent assemblies. Its function to extract the bit timing from the received signal remains unchanged in the modification to duobinary operation. However, there is a significant modification in the required outputs, in that data and phase quantizer outputs are needed for both the I channel and the Q channel. A Q-channel phase integrator presently does not exist. Furthermore, 3-bit quantizing is not adequate for the duobinary Viterbi algorithm demodulator. Simulations of SQPSK transmitted through the zero-phase, maximally-flat filters show the effect of soft decision quantizing (1.5 dB degradation from ideal $\triangle$PSK with 3-bit quantizing at E_b/N_o = 8 dB; negligible degradation with 4-bit quantizing).

The first modification to the Receive Bit Synchronizer is to provide a Q-channel Phase Integrator (duplicate of A2A10), a Q-Channel Phase Dump Circuit (duplicate of A2A9), and a Q-Channel Phase Quantizer (duplicate of A2A8), since these do not presently exist. The necessary sampling clocks are internally available in the Q-Channel Timing and AGC (A2A30), which i a duplicate of A2A31. The Bit Sync Buffer (A2A29) and the Decoder Switch (A3A7) must be modified to accept the additional inputs.

To eliminate the excessive degradation of 3-bit quantizing, the Quantizer design (A2A8, A2A4, A2A32, and new assembly for Q channel) should be modified to perform 4-bit quantizing, although this is not absolutely necessary. The Bit Sync Buffer (A2A29) and the Decoder Switch (A3A7) must be modified to accept the additional inputs (4 lines instead of 3, for each quantity).

The I Channel Timing and AGC (A2A31) and Q Channel Timing and AGC (A2A30) should be modified in the AGC circuit. Presently, a binary decision is made whether the absolute value of the input voltage to the AFC circuit exceeds a reference level (defined here as 1.0). Hence, the AFC stabilizes when the reference level is exceeded 50 percent of the time. The preferred modification* is to have a tertiary decision, the third being a null output when the absolute value of the input voltage is less than half the reference level (0.5).

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*With random data, an alternate simpler modification sets the two levels of the binary decision to be unequal so that 1.0 amplitude is exceeded 25 percent of the time. The MD-1002 is currently being modified to incorporate a data randomizer.
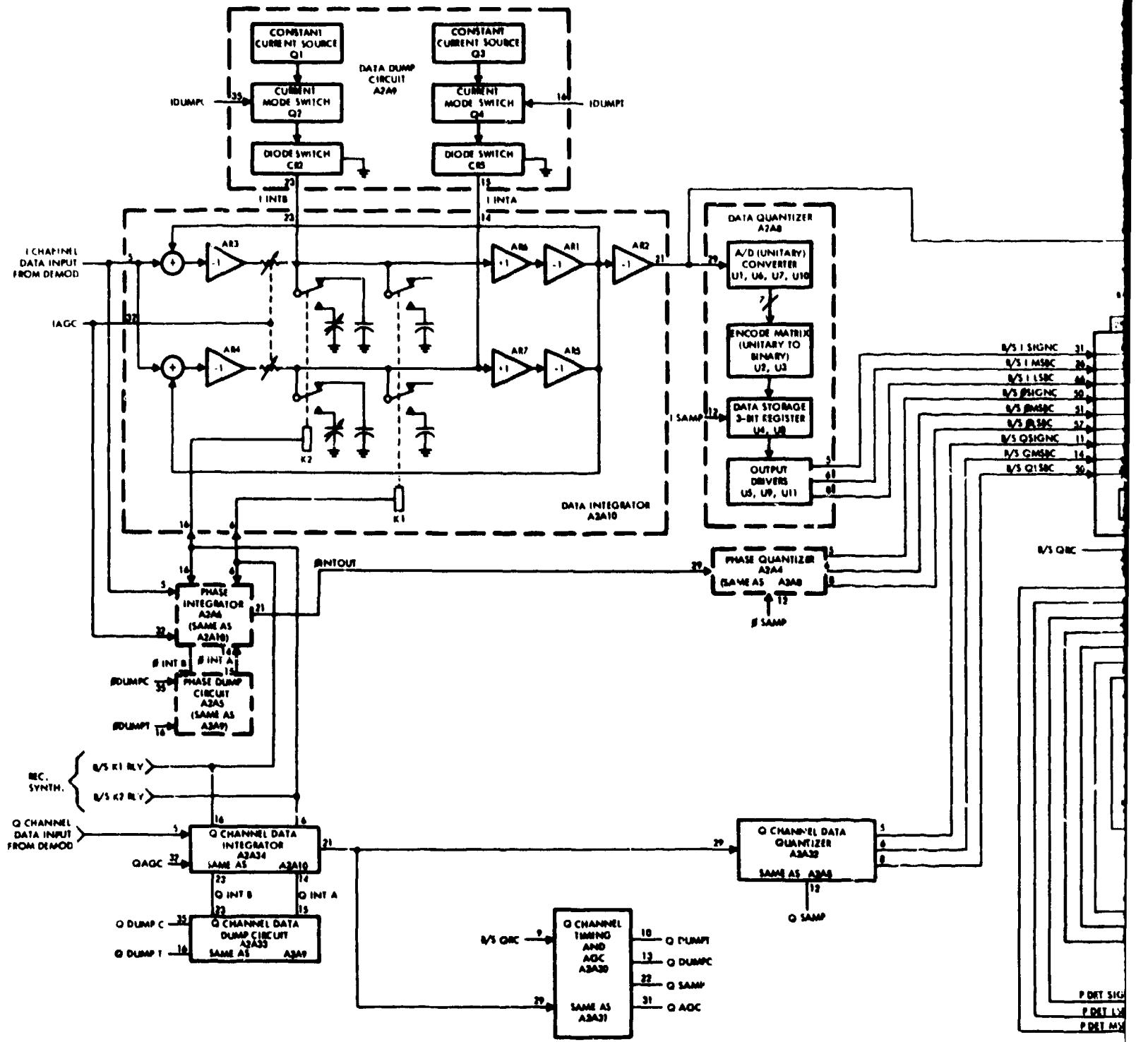
877-3780
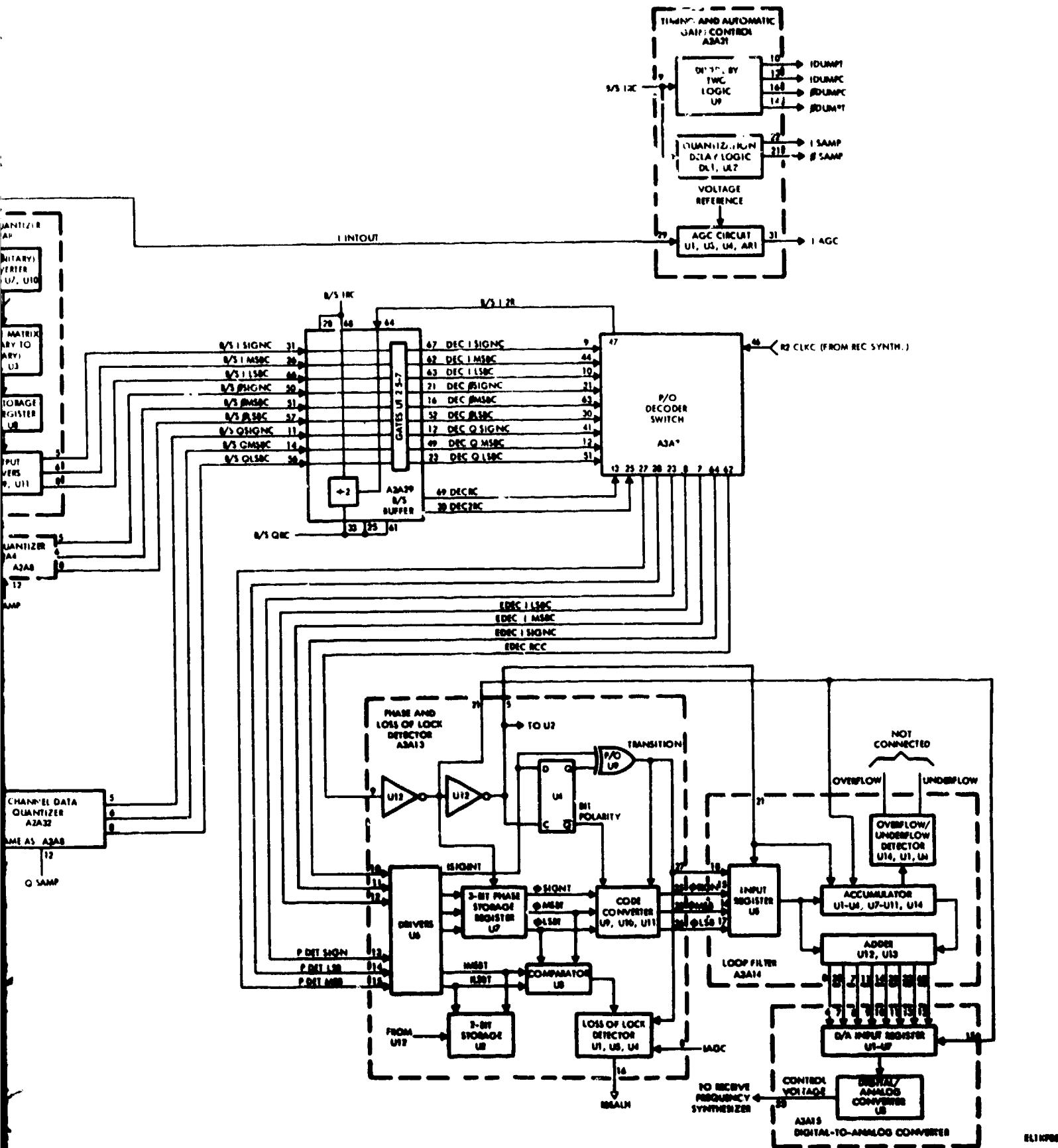
Figure D-4. Functional Block Diagram
of Receive Bit Synchronizer, FO-36

D-7

The input voltage to the I Channel Timing And AGC (A2A31) should be derived from the I Channel Phase Integrator (A2A6), rather than from A2A10. The input voltage to the Q Channel Timing And AGC (A2A32) should be derived from the Q Channel Phase Integrator (New Assembly), rather than from A2A34.

D.4 COMPLETELY NEW ASSEMBLIES FOR CARRIER TRACKING AND SYNC DETECTION

Figure D-2 contains two completely new functions for carrier tracking and sync detection. Let us assume these will be individual assemblies which accept the I and Q Phase and Data Integrator samples available from the Receive Bit Synchronizer. The functional requirements for these assemblies are now discussed. Since the Receive Bit Synchronizer outputs quantized soft decisions on the I and Q samples, a digital implementation of the functions may be appropriate.

The Receive Bit Synchronizer (modified) outputs 4-bit quantized decision on I Phase, I Data, Q Phase and Q Data. The soft decisions on I Phase and Q Phase are accepted by the Duobinary Viterbi Algorithm, while I Data and Q Data are needed only for the tracking functions.* Timing for Q Data is aligned with I Phase, while Q Phase is aligned with I Data, because of the staggered QPSK modulation.

The Decision-Directed Carrier Tracking Error assembly functions as follows (at the I-channel symbol rate):

I Phase and Q Phase Are hard duobinary quantized,

Set to +1 If $> .5$
Set to 0 If $> -.5$ and $< .5$
Set to -1 If $> -.5$

Multiply hard-quantized I Phase By soft-quantized Q Data
Multiply hard-quantized Q Phase By soft-quantized I Data
Subtract and output result As DC voltage to A2A24 (modified to accept DC error voltage input).

Note that hard duobinary quantizing is a simple logic conversion from the 4-bit soft quantizing.

---

*In the conventional operation of the modem, the data bits are extracted from I Data and Q Data.

The Sync Zone Detector processes the I Phase and Q Phase soft decisions. Sync is declared when a large fraction of these decisions are close to the ideal duobinary hard decision values, -1, 0, 1. The narrow amplitude region about these ideal values is defined as the sync zone. Note that if the soft decision quantizer covers a range slightly greater than -1 to +1, the sync zone detector can be a simple code conversion on the soft decisions. As an example, let the quantizer have 16 levels from -1.25 to +1.25, with a spacing of 0.1667. The sync zone can be declared as the quantizing levels closest to the ideal values, -1, 0, 1. There are 6 such levels, out of the total of 16. This defines the sync zone to be of width ± 0.1667 about the ideal values.

The Sync Zone Detector assembly functions as follows (at the I-channel symbol rate):

  Set output to +2 if both I Phase and Q Phase fall into the sync zone.
  Set output to 0 if either but not both falls into the sync zone.
  Set output to -2 if neither falls into the sync zone.
  The output voltage drives pin P2-23 of A2A19.

This logic is a code conversion on the 4-bit quantized soft decisions made on I Phase and Q Phase.

Since the Sync Zone Detector recognizes the simultaneous occurrence of carrier phase lock and bit synchronization, the Loss Of Lock Detector within A3A13 can be eliminated. The output to the front panel can be obtained, instead, from the sync zone detector.

D.5 DUOBINARY VITERBI ALGORITHM

The Duobinary Viterbi Algorithm for duobinary functions independently in parallel for I and Q. The 4-bit soft decisions on I Phase or Q Phase are input to the Duobinary Viterbi Algorithm, which is defined by the flowchart in Figure 2-5. The metrics can be integer quantized in the implementation of the flowchart, since there are 8 positive and 8 negative input levels with 4-bit quantizing of the input.

For purposes of discussion, assume the Duobinary Viterbi Algorithm is interfaced with the modem like an external decoder (although it may be more convenient to locate the algorithm inside the modified modem). Figure D-5 is a functional block diagram of the Decoder and Interface. Modification of the Decoder

EDECRCT 41
EDECRCT 42
EDECISIGN 27
EDEQSIGN 16
EDECIMSBC 28
EDECILSBC 15
EDECQMSBC 8
EDECQLSBC 5

INVERT
SWITCH
S2

U1
U3
U1
U3
U4
U4
U7
U7

TO PHASE
AND LOSS OF
LOCK
DETECTOR
A3A13

TO
METER
D/A CARD
A3A11

EDEC2RC

64 63 62

31 48 64 6 7 8 13 16   57 15 24

DEC2RC   29   U1&U2   U1
DEC 1C   43
DECISIGNC   9
DECQSIGNC   41
DECIMSBC   44
DECILSBC   10
DECQMSBC   12
DECQLSBC   51
DECISIGNC   21
DECQMSBC   63
DECQLSBC   20

FROM
BIT
SYNC
BUFFER
A2A29

INPUT CLOCK
GATE
U10

INPUT DATA
GATE
U10

INPUT DATA
GATE
U11

INPUT DATA
GATE
U11

INPUT DATA
GATE
U12

INPUT DATA
GATE
U12

INPUT DATA
GATE
U13

INPUT DATA
GATE
U13

INPUT DATA
GATE
U14

INPUT DATA
GATE
U14

U5

SWITCHING
LOGIC
U2, U5

QPSK DATA GATE
AND MULTIPLEX
U7

BPSK DATA
GATE U3

CLOCK
SELECTOR
U3

DIFFERENTIAL
DECODER
U3, U4, U6, U9

U8

U8

OUTPUT
CIRCUIT
U6,

FROM RECEIVE
REFERENCE DIVIDER   R2CLKC   46   U1   6/U2R

DECODER S

677-3761

Figure D-5. Functional Block Diagram of Decoder and Interface, FO-44

Switch (A3A7) to accept 4-bit quantizing and the addition of a Q Phase Quantizer (New Assembly) has been mentioned above. As seen from Figure D-5, the Decoder Interface (A3A28) must be modified to output 4-bit quantizing. Furthermore, the connections from A3A7 to A3A28 must be modified to transfer I Phase and Q Phase soft decisions. An additional modification is that the Duobinary Viterbi Algorithm sends back I and Q data in parallel to A3A7 and these should input the QPSK Data Gate and Multiplex U7, in place of the I Sign and Q Sign bits from the Bit Sync Buffer through U10 and U11.

D.6   CONCLUSIONS

Modifying the Harris MD-1002 modem to duobinary SQPSK operation is technically feasible, but the required modifications are extensive.

APPENDIX E
## CONSIDERATIONS ON RATE-3/4 CODED CONVENTIONAL SQPSK OPERATION

This appendix discusses possible system modifications which would enable the Harris MD-1002 modem to operate with external rate-3/4 convolutional encoding/Viterbi decoding. It is desired to maintain the same interfaces as for rate-1/2 operation with the Linkabit KY-801 coder; e.g., data source → modem transmitter → encoder → modem transmitter → channel → modem receiver → decoder → modem receiver → data sink. In this interface plan, the modem acquires clock from the data source and supplies clock to the external coder on the basis of coded symbol rate being equal to twice the data rate (for rate-1/2 coding). The I and Q symbols are on parallel lines for SQPSK operation, which is the only mode examined here.

The basic approach to convert a rate-1/2 convolutional code to rate-3/4 has been described in the Phase A Final Report. It involves a repetitive pattern of symbol deletions (2 out of 6) from the rate-1/2 encoder output. The deleted symbols are restored as zero-amplitude erasures at the rate-1/2 decoder input. Simulations show that rate-3/4 performance is approximately 1 dB degraded from rate-1/2 over the ideal conventional binary PSK channel.

E.1 MD-1002 MODEM CONSIDERATIONS

The MD-1002 modem Technical Manual[11] gives information on the interface between this modem and an external coder. This interface for rate-1/2 coding is first reviewed.

Figure E-1 is a functional block diagram of the Encoder and Interface in the modem. The Transmit Bit Synchronizer within the modem acquires the input clock of data rate R and also generates a 2R clock. The differentially encoded data and these two clocks are sent to the external encoder, which sends back the coded I and Q symbols (in parallel) and the clock 2R. The I and Q symbols are gated at the 2R clock so that the offset needed for SQPSK operation is accomplished in the modem. The I and Q symbols and the 2R clock returned from the external encoder are sent to the RF Modulator portion of the modem.

ENCODER INTERFACE (A3A27)

50

P/O TEST
INTERFACE
(A3A8)

24

U4

60

27

51

12

7

10

22

U4

OFFSET
GATE
U16, U9

U4

2X CLOCK   11

DIFF
ENCODER
SWITCH   6

BPSK/QPSK
GATE
U14

STD/CLK/ICF SWITCH   9
BYPASS DATA   8
DATA   5

INPUT DATA
GATES
U1

DIFFERENTIAL
ENCODER
U7, U8

BPSK ENABLE
GATES
U6, U10

CLOCK   46

U4

÷2
U8

DATA DEMULTIPLEXER
AND DIFFERENTIAL
CODER U13

QPSK
ENABLE GATES
U13, U14

PN SEQUENCE   23
PN SEQUENCE   25
24

PN SEQUENCE
ENABLE GATE
U10

EXT CODER SWITCH   15
ENMODO   16

SWITCHING
LOGIC
U4, U11

CLOCK CONTROL   39
2R CLOCK   3
R CLOCK   41

CLOCK
GATE U5

÷2
U9

35
PN SEQUENCE CLOCK   71

BPSK/QPSK SWITCH   13

677-3782

Figure E-1. Encoder and Interface, FO-15

Thus, the data clock and the transmit symbol rate are distinct within the modem transmitter when an external coder is utilized.

Figure E-2 is a functional block diagram of the Decoder and Interface in the modem. The Receive Bit Synchronizer within the modem acquires the received symbol rate and generates the clock R. (The clock 2R is also generated, but this is not an external interface.) With rate-1/2 coding and SQPSK operation, the I symbol rate or Q symbol rate equals the data rate. The Receive Bit Synchronizer eliminates the offset between I and Q symbols, and the soft decisions for the coded symbols are sent in parallel to the external decoder, along with the clock R. The decoder sends back data and the clock R to the modem. Finally, the differentially-decoded data and the clock R from the external decoder are output from the modem.

The modem symbol rate and the output data rate are distinct within the modem receiver when an external coder is utilized.

On the basis of the above review, it is concluded that without any modification, the modem would be compatible with an external rate-3/4 coder at the data rate R provided that the coder generates the necessary clock conversions. The encoder receives the clock 2R from the modem, and must generate a new clock $2R' = (4/3)R$ which is returned to the modem along with the encoded I and Q symbols the rate R'). The decoder receives the I and Q soft decisions and the clock R' the modem, and must generate a new clock $R = (3/2)R'$, which is returned to modem along with the data.

If the external coder is not capable of these clock conversions, the alter ative is to modify the modem to generate $2R' = (4/3)R$ in the Transmitter Fr ency Synthesizer (which is locked to the data rate R) and the rate $R = (3/2)R'$ in the Receive Frequency Synthesizer (which is locked to the receive symbol rate R'). In addition, the modem would have to have these new clocks appropriately available on the connector to the external coder.

E.2   USE OF AN INTERFACE BOX BETWEEN UNMODIFIED MD-1002 MODEM AND UNMODIFIED KY-801 CODER TO ENABLE RATE-3/4 OPERATION

Since the KY-801 can be converted to rate-3/4 operation by a repetitive deletion pattern, and the MD-1002 is compatible with an external rate-3/4 coder with appropriate clock conversions, an interface box in the connection between the modem and the coder is a possible approach to implement rate-3/4 operation with unmodified modems and rate-1/2 coders.
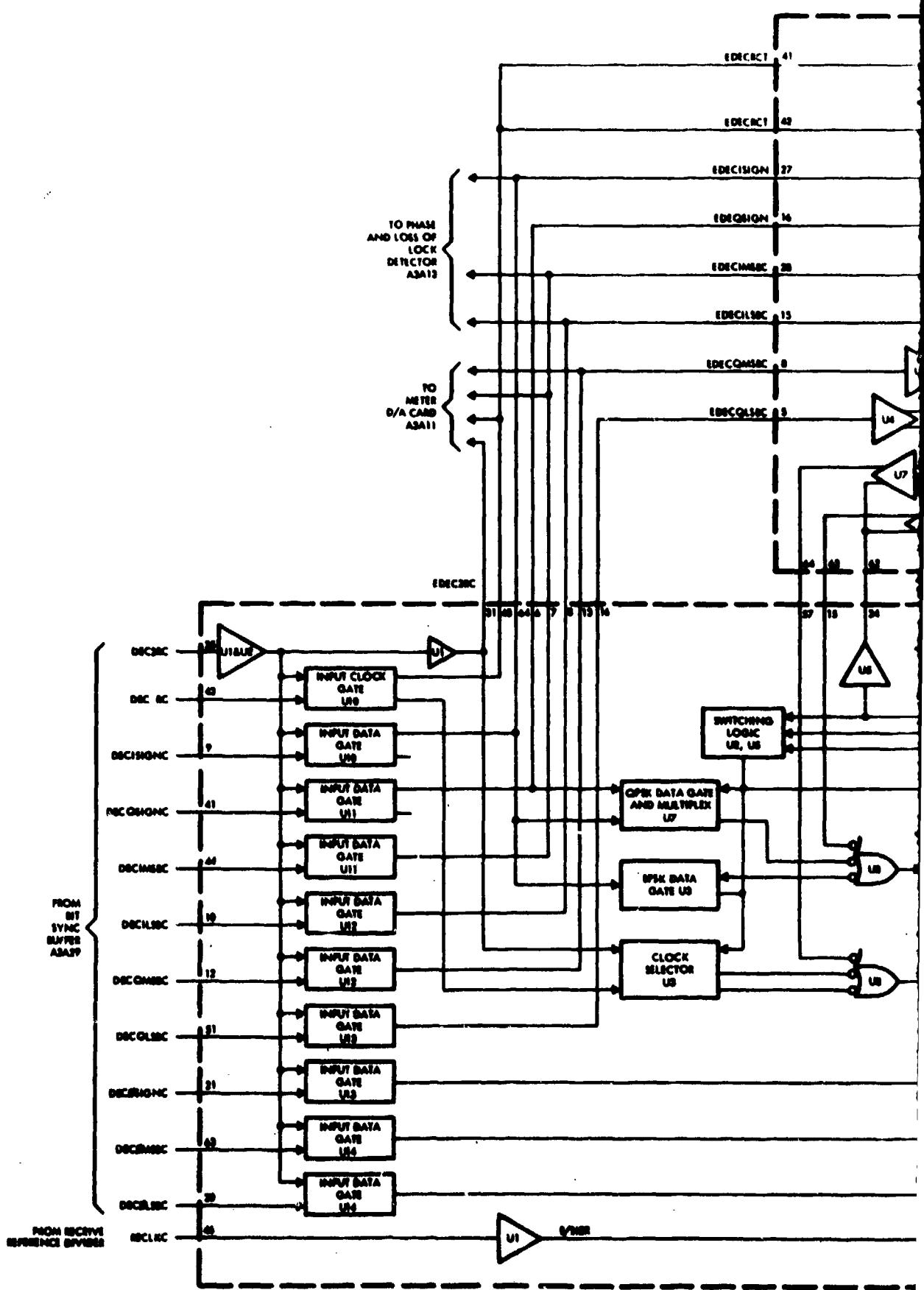
877-3781
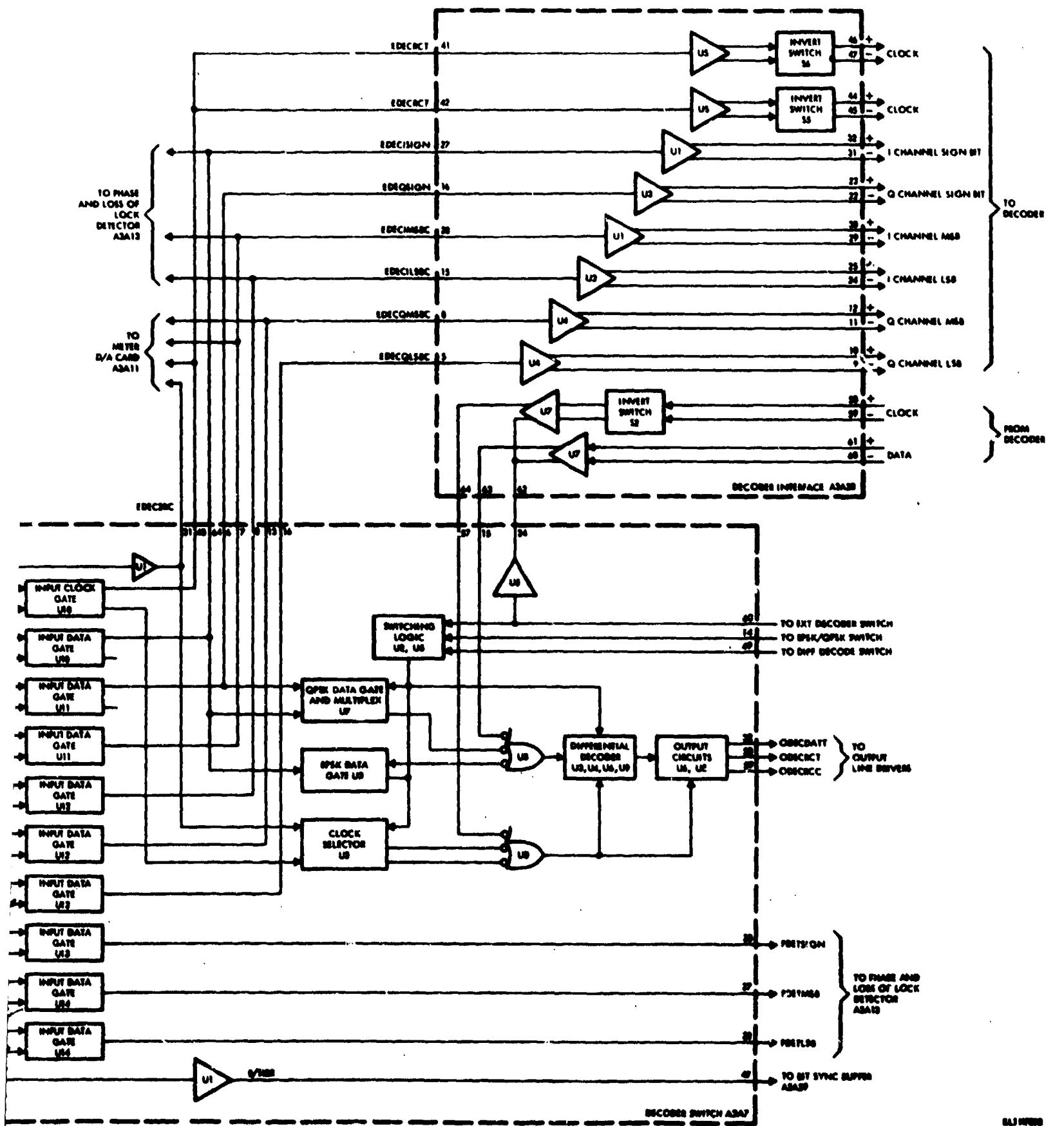
Figure E-2. Decoder and Interface, FO-44

The encoder/modem transmitter interface functions as follows:

> The clock from the encoder at rate 2R is converted by
> the interface to $2R' = (4/3)R$. Successive groups of 6
> symbols are generated at symbol rate 2R by the encoder.
> In each group, two symbols are deleted by the interface,
> and the remaining 4 symbols (2, 3, 5, 6) are sent to the modem
> at rate 2R'. Clock 2R' is sent back to the modem from the
> interface.

The decoder/modem receiver interface functions as follows:

> The clock from the modem at rate R' is converted to
> $R = (3/2)R'$.
>
> Starting at an arbitrary point in the symbol stream,
> the two deleted symbols (1, 4) in each group of 4
> symbols from the modem are restored as erasures;
> i.e., as minimum amplitude soft decisions with
> random sign bits.
>
> The 6 restored symbols are sent to the decoder in I,
> Q pairs at rate R.
>
> The data is returned to the modem at rate R together
> with the clock R.
>
> The sync state of the decoder is sent to the interface.
> After several changes in sync state, indicating that
> the decoder is not synchronized, the starting point is
> assumed to be incorrect and is advanced to the next
> symbol. (Note, if the starting point is on a Q symbol,
> the Q sign bits are complemented to compensate for the
> 90° phase shift in the modem.)

Figure E-3 illustrates this interface. The decoder's sync state is already available on the coder connector, according to discussions with Linkabit. A solid line through the interface box means that signal is not actually used within the interface.
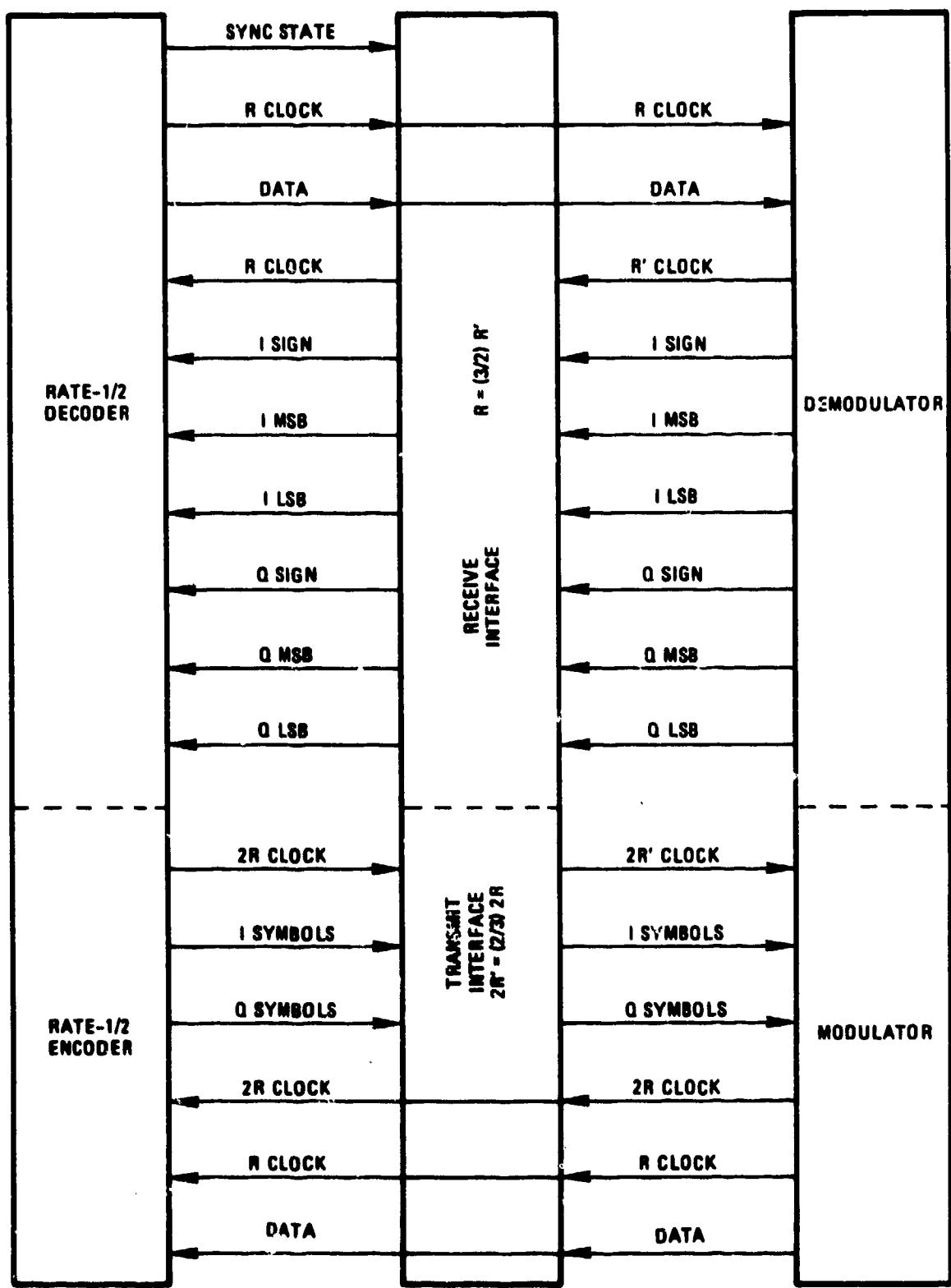
677-3763

Figure E-3. Interface for Rate-3/4 SQPSK With Unmodified MD-1002 and Unmodified KY-801

E.3   RATE-3/4 PERFORMANCE WITH INTERFACE BOX

A significant performance disadvantage is incurred using the interface approach of Figure E-3. The problem is that the rate-3/4 performance depends on being able to restore the deleted symbols at exactly zero amplitude. Unfortunately, this is not possible with the 3 bit sign/magnitude quantization for soft decisions to the KY-801. Consequently, the erasures can be restored only at the lowest magnitude, with a randomly selected sign bit.

It is understood that the KY-801 assigns the metric values 1, 2, 3, 4 to the four possible quantized amplitudes (not considering sign). Simulation of rate-3/4 operation over an ideal PSK channel with this quantization, setting the threshold spacing of the quantizer at half the rms noise but restoring the erasures at zero amplitude gives results close to the unquantized results. However, when the erasures are restored at the minimum amplitude with a random sign bit, the performance is found to be degraded by approximately 2 dB.

A plausible explanation of this severe degradation is found from the distance properties of the constraint-length 7, rate-1/2 convolutional code. The minimum distance of the code is 10; i.e., an incorrect code word differs from the correct word in at least 10 symbols. After deleting symbols to create a rate-3/4 code, the minimum distance is reduced to 5. Therefore, when the Viterbi decoder compares the metric for the correct word with the metric for an incorrect word at distance 5, the metric difference must also include the contribution from $10 - 5 = 5$ erasures. At threshold E_b/N_o, the variance of an erasure restored at minimum amplitude with random sign (instead of at zero amplitude) is found to be comparable with the variance of a quantized soft decision; hence, by this argument, the degradation is predicted to be approximately 3 dB.

E.4   CONCLUSIONS

It is feasible to develop an interface box enabling rate-3/4 SQPSK operation with unmodified MD-1002 modems and unmodified KY-801 coders. The interface deletes symbols from the encoder and restores them as erasures to the decoder. The major design difficulty is obtaining the necessary 3/2 and 2/3 clock conversions for any data rate over the wide operating range of the modem, 50 Kbps to 10 Mbps. However, performance is not satisfactory with this approach because the decoder cannot accept a zero amplitude restoration of the erased symbols.

One solution would be to modify the decoder so as to accept zero amplitude (i.e., null zone) soft decisions. Then, the erased symbols can be properly restored at zero amplitude. It may be preferable, then, to include the entire interface within the modified coder, which would need a control to select rate-1/2 or rate-3/4 operation. Then, the external coder is rate-3/4, but with compatible interfaces to operate with the unmodified MD-1002 modem.

Another possibility is to modify both the modem and the coder. The modem modification consists of extracting a $(4/3)R$ clock from the transmit frequency synthesizer and a $(3/2)R'$ clock from the receive frequency synthesizer to be delivered to the external coder, with a control to select rate-1/2 or rate-3/4 operation. The coder modification now is simpler because it does not need to include clock conversion.

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